Si5381/82 Rev. E Reference Manual

Overview

This Reference Manual is intended to provide system, PCB design, signal integrity, and software engineers the necessary technical information to successfully use the Si5381/82 devices in end applications. The official device specifications can be found in the Si5381/82 datasheet.

The Si5381/82 is a high performance jitter attenuating clock multiplier which integrates four/two any-frequency DSPLLs for applications that require maximum integration and independent timing paths. A single low phase noise XO connected to the XA/XB input pins provides the reference for the device. The device supports ultra-low phase noise 4G/LTE clock generation and low jitter general-purpose clock synthesis from a single device. Each DSPLL has access to any of the four inputs and can provide low jitter clocks on any of the device outputs. Based on fourth generation DSPLL technology, these devices provide any-frequency conversion with typical jitter performance under 100 fs (4G/LTE frequency outputs). Each DSPLL supports independent free-run, holdover modes of operation, as well as automatic and hitless input clock switching. The Si5381/82 is programmable via an SPI or I^2C serial interface with in-circuit programmable non-volatile memory so that it always powers up in a known configuration.

RELATED DOCUMENTS

- Si5381/82 Data Sheet
- Si5381/82 Device Errata
- Si5381/82A-E-EVB User Guide
- Si5381/82A-E-EVB Schematics, BOM & Layout
- IBIS models
- To download evaluation board design and support files, go to: http://www.silabs.com/Si538x-4x-EVB
- JESD204B subclass 0 and subclass 1 support

Work Flow Expectations with ClockBuilder™ Pro and the Register Map

This reference manual is to be used to describe all the functions and features of the parts in the product family with register map details on how to implement them. It is important to understand that the intent is for customers to use the ClockBuilder™ Pro software to provide the initial configuration for the device. Although the register map is documented, all the details of the algorithms to implement a valid frequency plan are fairly complex and are beyond the scope of this document. Real-time changes to the frequency plan and other operating settings are supported by the devices. However, describing all the possible changes is not a primary purpose of this document. Refer to Applications Notes and Knowledge Base article links within the ClockBuilder Pro GUI for information on how to implement the most common, real-time frequency plan changes.

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1. Functional Description

The Si5381/82 integrates four/two independent any-frequency DSPLLs in a monolithic IC for applications that require a combination of 4G/LTE, wireline, and general-purpose clocking. Any clock input can be routed to any DSPLL. The output of any DSPLL can be routed to any of the device clock inputs. Based on 4th generation DSPLL technology, the Si5381/82 provides a clock-tree-on-a-chip solution for applications that need a mix of 4G/LTE and general-purpose frequencies.

1.1 DSPLL

The DSPLL provides the synthesis for generating the output clock frequencies which are synchronous to the selected input clock frequency or freerun from the reference clock. It consists of a phase detector, a programmable digital loop filter, a high-performance ultra-low-phase-noise analog VCO, and a user configurable feedback divider. Use of an external XO provides the DSPLL with a stable low-noise clock source for frequency synthesis and for maintaining frequency accuracy in the Freerun or Holdover modes. No other external components are required for oscillation. A key feature of DSPLL is providing immunity to external noise coupling from power supplies and other uncontrolled noise sources that normally exist on printed circuit boards.

The frequency configuration for each of the DSPLLs is programmable through the SPI or I^2C interface and can also be stored in non-volatile memory. DSPLLB is primarily used to generate 4G/LTE frequencies. Fractional frequency multiplication (Mn/Md) allows each of the DSPLLs to lock to any input frequency and generate virtually any output frequency. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

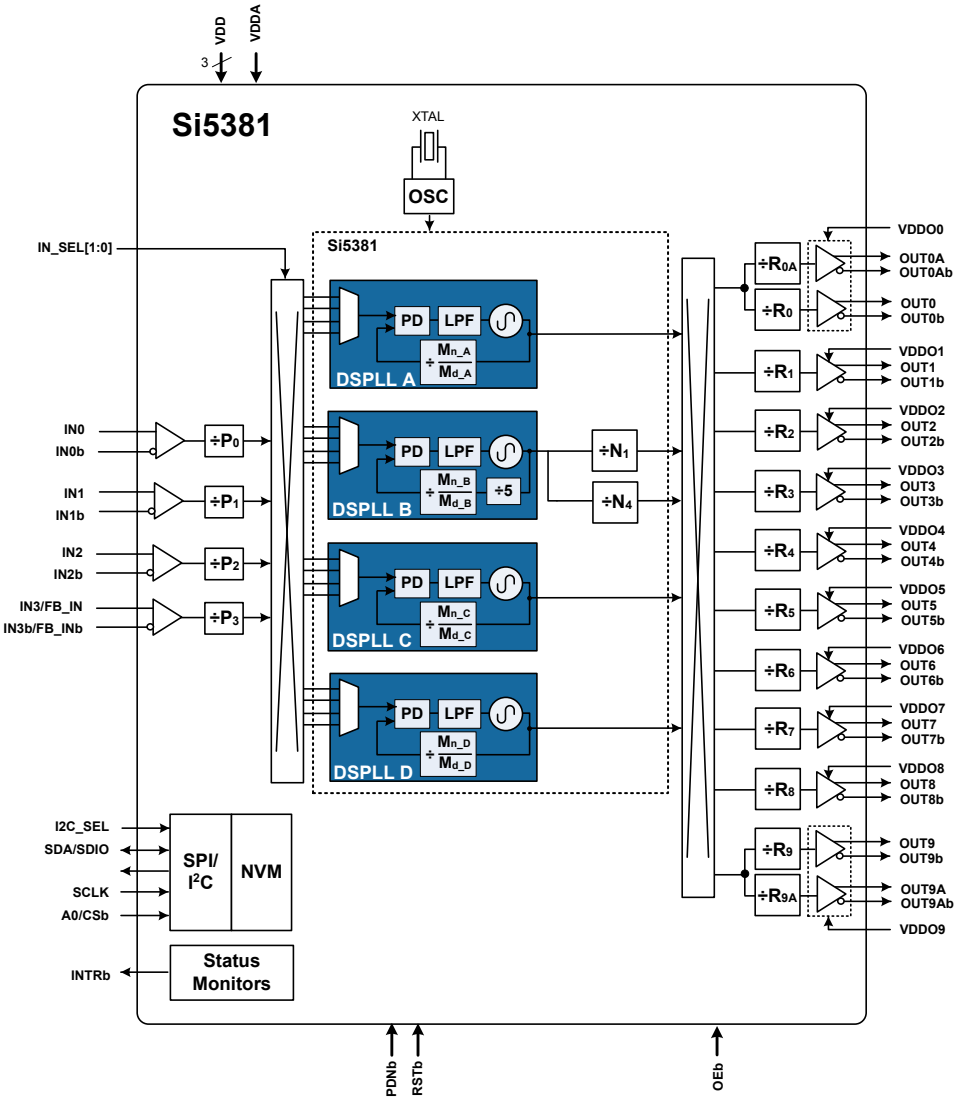


Figure 1.1. Si5381 Block Digram

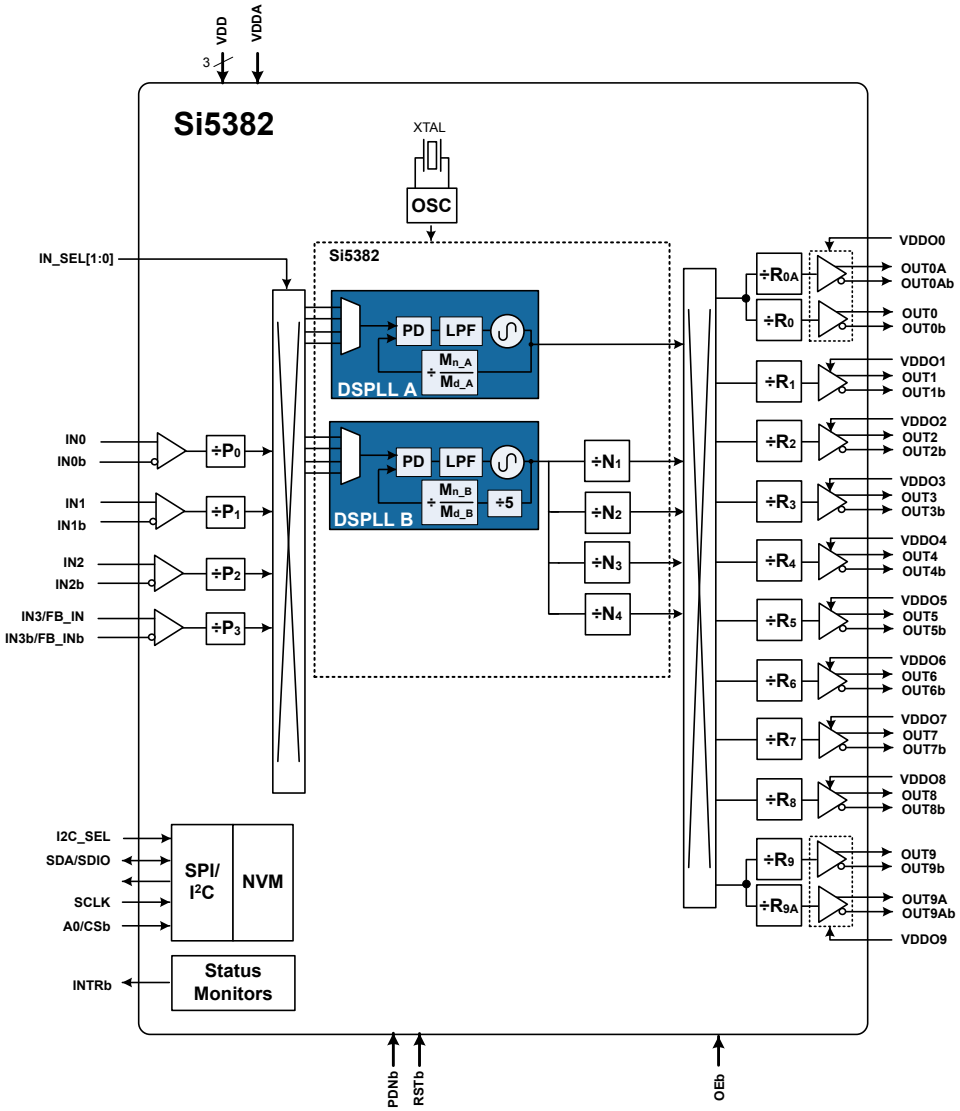


Figure 1.2. Si5382 Block Digram

1.2 Si5381/82 LTE Frequency Configuration

The device's frequency configuration is fully programmable through the serial interface and can also be stored in non-volatile memory. The combination of flexible integer dividers and a high frequency VCO allows the device to generate multiple output clock frequencies for applications that require ultra-low phase noise and spurious performance. The table below shows a partial list of possible output frequencies for LTE applications. Note that these 4GE/LTE frequencies may be generated with an Ethernet input clock to DSPLL B. These frequencies are distributed to the output dividers using a configurable crosspoint mux. The output R dividers allow further division for up to 12 unique integer-ratio related frequencies on the Si5381/82. The ClockBuilder Pro software utility provides a simple means of automatically calculating the optimum divider values (P, M, N and R) for the frequencies listed in the table below. In addition to the LTE frequencies, the Si5381/82 devices can simultaneously generate wireline clocks like 156.25 MHz, 155.52 MHz, 125 MHz, etc. and system clocks like 100 MHz, 33 MHz, 25 MHz, etc.

Table 1.1. Example List of Possible 4G/LTE Clock Frequencies

Example 4G/LTE Device Clock Frequencies Fout (MHz)
15.36
19.20
30.72
38.40
61.44
76.80
122.88
153.60
184.32
245.76
307.20
368.64
491.52
614.40
737.28
938.04
1228.80
1474.56
1638.4
1843.2
2106.51428571
2457.6
2949.12

1.3 Si5381/82 Configuration for JESD204B subclass 1 Clock Generation

The Si5381/82 can be used as a high-performance, fully-integrated JEDEC JESD204B jitter cleaner while eliminating the need for discrete VCXO and loop filter components. The Si5381/82 supports JESD204B subclass 0 and subclass 1 clocking by providing both device clocks (DCLK) and system reference clocks (SYSREF). The 12 clock outputs can be independently configured as device clocks or SYSREF clocks to drive JESD204B ADCs, DACs, FPGAs, or other logic devices. The Si5381/82 will clock up to six JESD204B subclass 1 targets, using six DCLK/SYSREF pairs. If SYSREF clocking is implemented in external logic, then the Si5381/82 can clock up to 12 JESD204B targets. Not limited to JESD204B applications, each of the 12 outputs is individually configurable as a high performance output for traditional clocking applications.

For applications which require adjustable static delay between the DCLK and SYSREF signals, the Si5381/82 supports up to four DCLK/SYSREF pairs, each with independently adjustable delay. An example of an adjustable delay JESD204B frequency configuration is shown in the following figure. In this case, the N0 divider determines the device clock frequencies while the N1-N4 dividers generate the divided SYSREF used as the lower frequency frame clock. Each output N divider also includes a configurable delay (Δt) for controlling deterministic latency. This example shows a configuration where all the device clocks are controlled by a single delay (Δt0) while the SYSREF clocks each have their own independent delay (Δt1 -Δt4), though other combinations are also possible. The bidirectional delay is programmable over ±8.6 ns in 68 ps steps. See Output Delay Control (Δt0 -Δt4) for more information on delay control. The SYSREF clock is always periodic and can be controlled (on/off) without glitches by enabling or disabling its output through register writes.

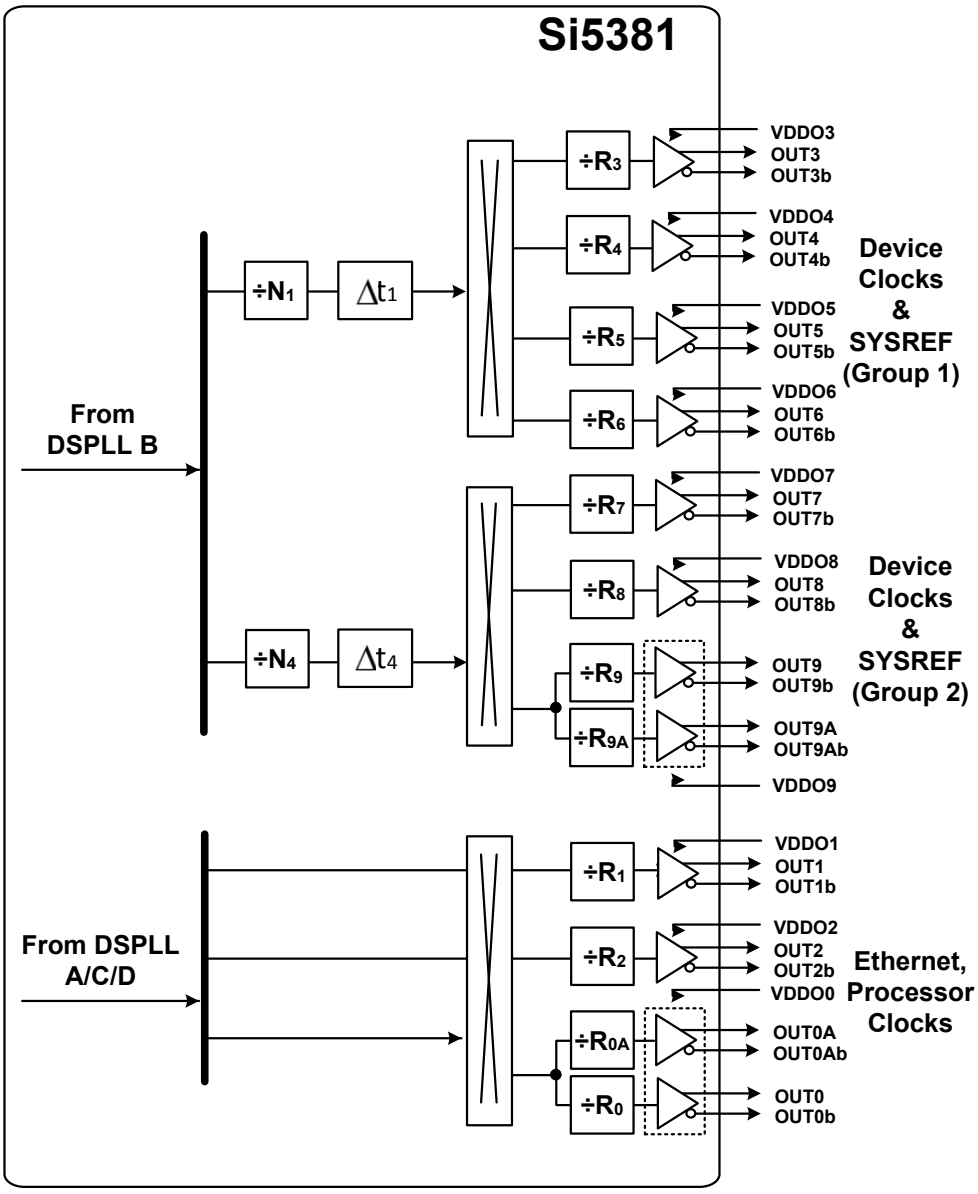


Figure 1.3. Example Si5381 Divider Configuration for Generating JESD204B Subclass 1 Clocks

1.4 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation and wander filtering. Register configurable loop bandwidth settings in the range of 1 Hz to 4 kHz are available for selection. Since the loop bandwidth is controlled digitally, each DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection. The DSPLL loop bandwidth register values are determined using ClockBuilder Pro. Note that after manually changing bandwidth parameters, the BW_UPDATE_PLLx bit must be set high to latch the new values into operation. This update bit will latch the new values for Loop, Fastlock, and Holdover Exit bandwidths simultaneously.

Table 1.2. DSPLL Loop Bandwidth Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
BW_PLLA	0408[5:0] - 040D[5:0]	0408[5:0] - 040D[5:0]	This group of registers determines the loop bandwidth for DSPLL A, B, C, D. The loop bandwidth can be from 1 Hz to 4 kHz. Register values are automatically determined by ClockBuilder Pro.
BW_PLLB	0508[5:0] - 050D[5:0]	0508[5:0] - 050D[5:0]	
BW_PLLC	0608[5:0] - 060D[5:0]	—	
BW_PLLD	0709[5:0] - 070E[5:0]	—	
BW_UPDATE_PLLA	0x0414[0]	0x0414[0]	Writing a 1 to this register bit will latch Loop, Fastlock, and Holdover Exit BW parameter registers for DSPLL A.
BW_UPDATE_PLLB	0x0514[0]	0x0514[0]	Writing a 1 to this register bit will latch Loop, Fastlock, and Holdover Exit BW parameter registers for DSPLL B.
BW_UPDATE_PLLC	0x0614[0]	—	Writing a 1 to this register bit will latch Loop, Fastlock, and Holdover Exit BW parameter registers for DSPLL C.
BW_UPDATE_PLLD	0x0715[0]	—	Writing a 1 to this register bit will latch Loop, Fastlock, and Holdover Exit BW parameter registers for DSPLL D.

1.4.1 Fastlock

Selecting a low DSPLL loop bandwidth (e.g. 1 Hz) will generally lengthen the lock acquisition time. The Fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher Fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock bandwidth settings in the range from up to 4 kHz are available for selection. Fastlock bandwidth should generally be set from 10x to 100x the loop bandwidth for optimal results. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting. The Fastlock feature can be enabled or disabled independently by register control. If enabled, when LOL is asserted Fastlock will be automatically enabled. When LOL is no longer asserted, Fastlock will be automatically disabled. Note that after changing the bandwidth parameters, the BW_UPDATE_PLLx bit must be set to 1 to latch the new values into operation. Note that the BW_UPDATE_PLLx update bit will latch new values for Loop, Fastlock, and Holdover Exit bandwidths simultaneously.

Table 1.3. Fastlock Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
FASTLOCK_AUTO_EN_PLLA	042B[0]	042B[0]	Auto Fastlock Enable/Disable. 0: Disable Auto Fastlock (default) 1: Enable Auto Fastlock
FASTLOCK_AUTO_EN_PLLB	052B[0]	052B[0]	
FASTLOCK_AUTO_EN_PLLC	062B[0]	—	
FASTLOCK_AUTO_EN_PLLD	072C[0]	—	
FAST_BW_PLLA	040E[5:0] - 0413[5:0]	040E[5:0] - 0413[5:0]	Fastlock bandwidth is selectable in the range of 1 Hz up to 4 kHz. Register values determined using ClockBuilder Pro.
FAST_BW_PLLB	050E[5:0] - 0513[5:0]	050E[5:0] - 0513[5:0]	
FAST_BW_PLLC	060E[5:0] - 0613[5:0]	—	
FAST_BW_PLLD	070F[5:0] - 0714[5:0]	—	
FASTLOCK_MAN_PLLA	0x042B[1]	0x042B[1]	Force Fastlock for DSPLL A 0: Normal Operation (default) 1: Force Fastlock
FASTLOCK_MAN_PLLB	0x052B[1]	0x052B[1]	Force Fastlock for DSPLL B 0: Normal Operation (default) 1: Force Fastlock
FASTLOCK_MAN_PLLC	0x062B[1]	—	Force Fastlock for DSPLL C 0: Normal Operation (default) 1: Force Fastlock
FASTLOCK_MAN_PLLD	0x072C[1]	—	Force Fastlock for DSPLL D 0: Normal Operation (default) 1: Force Fastlock

The loss of lock (LOL) feature is a fault monitoring mechanism. Details of the LOL feature can be found in 3.3.4 DSPLL Loss-of-Lock (LOL) Detection.

1.4.2 Holdover Exit Bandwidth

In additional to the Loop and Fastlock bandwidths, a user-selectable bandwidth is available when exiting holdover and locking or relocking to an input clock when ramping is disabled (HOLD_RAMP_BYP = 1). CBPro sets this value equal to the Loop bandwidth by default.

Note that the BW_UPDATE_PLLx bit will latch new values for Loop, Fastlock, and Holdover bandwidths simultaneously.

Table 1.4. DSPLL Holdover Exit Bandwidth Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
HOLDEXIT_BW_PLLA	0x049D[5:0] – 0x04A2[5:0]	0x049D[5:0] – 0x04A2[5:0]	Determines the Holdover Exit BW for DSPLL A. Parameters are generated by ClockBuilder Pro.
HOLDEXIT_BW_PLLB	0x059D[5:0] – 0x05A2[5:0]	0x059D[5:0] – 0x05A2[5:0]	Determines the Holdover Exit BW for DSPLL B. Parameters are generated by ClockBuilder Pro.
HOLDEXIT_BW_PLLC	0x069D[5:0] – 0x06A2[5:0]	—	Determines the Holdover Exit BW for DSPLL C. Parameters are generated by ClockBuilder Pro.
HOLDEXIT_BW_PLLD	0x079D[5:0] – 0x07A2[5:0]	—	Determines the Holdover Exit BW for DSPLL D. Parameters are generated by ClockBuilder Pro.

1.5 Dividers Overview

There are four main divider classes within the Si5381/82. Additionally, FSTEPW can be used on DSPLLs A, C, and D to adjust the nominal output frequency in DCO mode. All M and N divisor values for the Si5381/82 may be Integer or Fractional. All P divisors used for inputs to DSPLL B must be Integer. P divisors used for other DSPLLs may be either Integer or Fractional. Refer to the corresponding block diagrams in 1.1 DSPLL to see the individual dividers.

- P0-P3: Input clock wide range dividers (0x0208-0x022F)
  - 48-bit numerator, 32-bit denominator
  - Min. value is 1, Max. value is 2^{24} (Fractional-P divisors must be > 5)
  - Practical P divider range of (Fin / 2 MHz) < P < (Fin / 8 kHz)
  - Each divider has an update bit that must be written to cause a newly written divider value to take effect.
  - Soft Rest All will also update the P divider values
  - DSPLL B in Si5381/82 devices requires integer P dividers. Fractional dividers can be used for all other DSPLLs.
- M: DSPLL feedback divider (0x0415-0x041F, 0x0515-0x051F, 0x0615-0x061F, 0x0716-0x0720)
  - 56-bit numerator, 32-bit denominator
  - Min. value is 5, Max. value is 2^{24} (Fractional-M divisors must be > 10)
  - Practical M divider range of (Fdco / 2 MHz) < M < (Fdco / 8 kHz)
  - The M divider has an update bit that must be written to cause a newly written divider value to take effect.
  - Soft Reset will also update M divider values.
  - DSPLL B includes an additional divide-by-5 in the feedback path. Manually calculated M divider register values must be adjusted accordingly.
- N: Output dividers (0x0302 - 0x0338)
  - 44-bit numerator, 32-bit denominator
  - Min. value is 5, Max. value is 2^{24} (Fractional-N divisors must be > 10)
  - Each N divider has an update bit that must be written to cause a newly written divider value to take effect.
  - Soft Reset will also update N divider values.
- R: Final output divider (0x0247-0x026A)
  - 24-bit field
  - Min. value is 2, Max. value is 2^{25}-2
  - Only even integer divide values: 2,4,6, etc.
  - R Divisor = 2 x (Field +1). For example, Field = 3 gives an R divisor of 8.
- FSTEPW: DSPLL DCO step words for DSPLLs A/C/D (0x0423-0x0429,0x0623-0x0629, 0x0724-0x072A)
  - Positive Integers, where FINC/FDEC selects direction
  - Min. value is 0, Max. value is 2^{24}
  - Only even integer divide values: 2,4,6, etc.
  - 56-bit step size, relative to 32-bit M numerator

2. Modes of Operation

After initialization, the DSPLL will operate in one of the following modes: Free-run, lock-acquisition, locked, or Holdover. These modes are described further in the sections below.

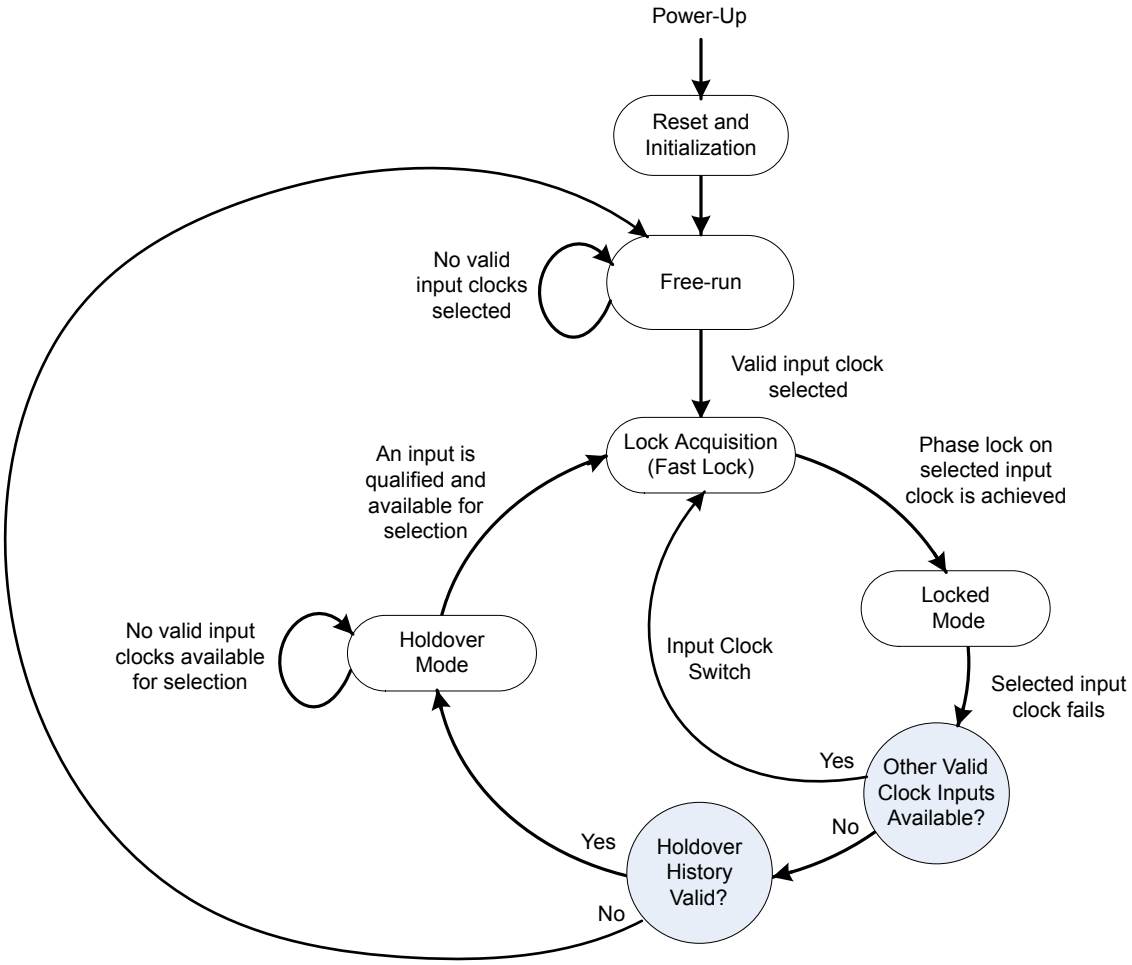


Figure 2.1. Modes of Operation

2.1 Reset and Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the SPI or I^2C serial interface is possible once this initialization period is complete. No output clocks will be generated until the initialization is complete.

There are two types of resets available. A Hard Reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits including the serial interface, will be restored to their initial state. A Hard Reset is initiated using the RSTb pin or by asserting the Hard Reset bit. A Soft Reset bypasses the NVM download and is used to initiate register configuration changes. A hard reset affects all DSPLLs, while a soft reset can affect all or each DSPLL individually. Also, any reset affecting DSPLL B will reset DSPLLs A/C/D as well. Individual DSPLL soft resets do not update the loop/fastlock bandwidths. If these settings have changed, they must be updated using BW_UPDATE_PLLx prior to issuing the individual soft reset.

Table 2.1. Reset Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
HARD_RST	001E[1]	001E[1]	Performs the same function as power cycling the device. All registers will be restored to their default values.
SOFT_RST_ALL	001C[0]	001C[0]	Resets the device without re-downloading the register configuration from NVM.
SOFT_RST_PLLA	001C[1]	001C[1]	Performs a soft reset on DSPLL A only.
SOFT_RST_PLLB	001C[2]	001C[2]	Performs a soft reset on DSPLL B only.
SOFT_RST_PLLC	001C[3]	—	Performs a soft reset on DSPLL C only.
SOFT_RST_PLLD	001C[4]	—	Performs a soft reset on DSPLL D only.

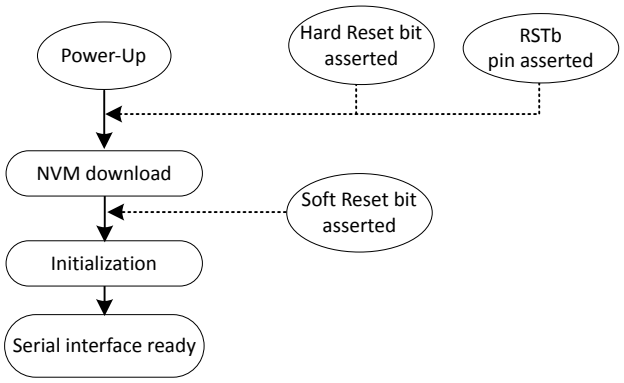


Figure 2.2. Initialization from Hard Reset and Soft Reset

The Si5381/82 is fully configurable using the serial interface (I^2C or SPI). At power up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD and VDDA pins.

2.1.1 Updating Registers During Device Operation

If certain registers are changed while the device is in operation, it is possible for the PLL to become unresponsive (i.e. lose lock indefinitely). Any change that causes the VCO frequency to change by more than 250 ppm since Power-up, NVM download, or SOFT_RST requires the following special sequence of writes. The following are the affected registers:

Control	Register(s)
P0_NUM / P0_DEN	0x0208 – 0x0211
P1_NUM / P1_DEN	0x0212 – 0x021B
P2_NUM / P2_DEN	0x021C – 0x0225
P3_NUM / P3_DEN	0x0226 – 0x022F
P0_FRACN_MODE / P0_FRAC_EN	0x0231
P1_FRACN_MODE / P1_FRAC_EN	0x0232
P2_FRACN_MODE / P2_FRAC_EN	0x0233
P3_FRACN_MODE / P3_FRAC_EN	0x0234
MXAXB_NUM / MXAXB_DEN	0x0235 – 0x023E
MXAXB_UPDATE	0x023F
Px_UPDATE	0x0230

PLL lockup can easily be avoided by using the following the preamble and postamble write sequence when one of these registers is modified during device operation. ClockBuilder Pro software adds these writes to the output file by default when Exporting Register Files.

1. To start, write the preamble by updating the following control bits using Read/Modify/Write sequences:

Register	Value
0x0B24	0xC0
0x0B25	0x04
0x0540	0x01

2. Wait 300 ms for the device state to stabilize.
3. Then modify all desired control registers.
4. Write 0x01 to Register 0x001C (SOFT_RST) to perform a Soft Reset once modifications are complete.
5. Write the postamble by updating the following control bits using Read/Modify/Write sequences:

Register	Value
0x0540	0x00
0x0B24	0xC3
0x0B25	0x06

2.1.2 NVM Programming

The NVM is two-time writable by the user. Once a new configuration has been written to NVM, the old configuration is no longer accessible.

While polling DEVICE_READY during the procedure below, the following conditions must be met in order to ensure that the correct values are written into the NVM:

- VDD and VDDA power must both be stable throughout the process.
- No additional registers may be written during the polling. This includes the page register at address 0x01. DEVICE_READY is available on every register page, so no page change is needed to read it.
- Only the DEVICE_READY register (0xFE) should be read during this time.

The procedure for writing registers into NVM is as follows:

1. Write all registers as needed. Verify device operation before writing registers to NVM.
2. You may write to the user scratch space (registers 0x026B to 0x0272) to identify the contents of the NVM bank.
3. Write 0xC7 to NVM_WRITE register.
4. Poll DEVICE_READY until DEVICE_READY=0x0F.
5. Set NVM_READ_BANK 0x00E4[0]=1.
6. Poll DEVICE_READY until DEVICE_READY=0x0F.

Alternatively, steps 5 and 6 can be replaced with a Hard Reset, either by RSTb pin, HARD_RST register bit, or power cycling the device to generate a POR. All of these actions will load the new NVM contents back into the device registers.

Note that the I2C_ADDR setting in register 0x000B is not saved as part of this NVM write procedure. To update this register in a non-volatile way, the "Si534x8x I2C Address Burn Tool" allows updating this value one time. This utility is included in the ClockBuilder Pro installation and can be accessed under the "Misc" folder in the installation directory.

Table 2.2. NVM Programming Registers

Register Name	Hex Address [Bit Field]	Function
ACTIVE_NVM_BANK	0x00E2[5:0]	Identifies the active NVM bank.
NVM_WRITE	0x00E3[7:0]	Initiates an NVM write when written with value 0xC7.
NVM_READ_BANK	0x00E4[0]	Download register values with content stored in NVM.
DEVICE_READY	0x00FE[7:0]	Indicates that the device is ready to accept commands when value = 0x0F.

2.2 Free Run Mode

Once power is applied to and initialization is complete, the DSPLL will automatically enter Freerun mode; generating the output frequencies determined by the NVM. The frequency accuracy of the generated output clocks in Freerun mode is entirely dependent on the frequency accuracy of the XAXB reference clock. Any temperature drift of this frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and lower wander while in Freerun or Holdover modes. Since there is little jitter attenuation from the XAXB pins to the clock outputs, devices should use a low-jitter XAXB reference clock to minimize output clock jitter.

2.3 Lock Acquisition Mode

The device monitors all inputs for a valid clock. If a valid clock is available for synchronization, the DSPLL will automatically start the lock acquisition process. If the Fastlock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

2.4 Locked Mode

Once locked, the DSPLL will generate output clocks that are both frequency and phase locked to its selected input clock. At this point, the XAXB reference clock frequency drift does not affect the output frequency. A loss of lock status bit indicates when lock is achieved. See 3.3.4 DSPLL Loss-of-Lock (LOL) Detection for more details on the operation of the loss of lock circuit.

2.5 Holdover Mode

Any of the DSPLLs will automatically enter holdover mode when the selected input clock becomes valid and no other valid input clocks are available for selection. Each DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. This delay value allows recent frequency information to be ignored for Holdover in cases where the input clock source frequency changes as it is removed.

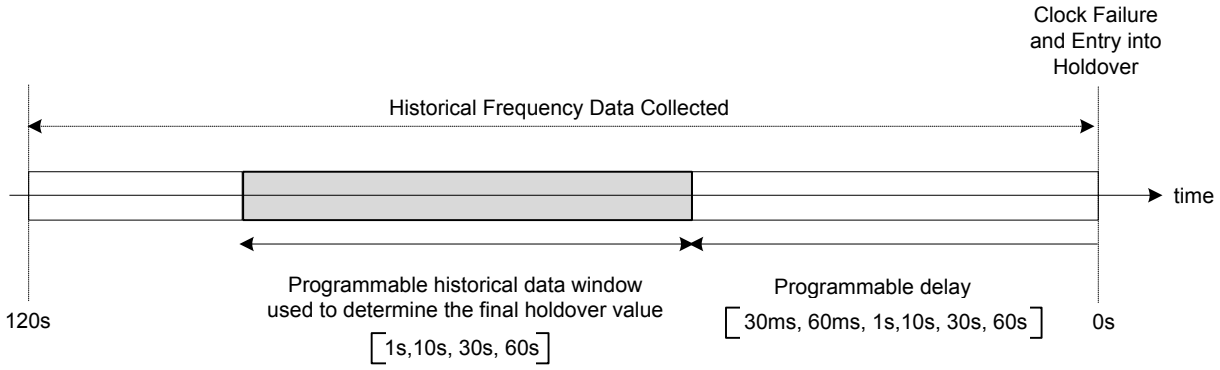


Figure 2.3. Programmable Holdover Window

When entering holdover, a DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is determined by the reference clock temperature drift. If a clock input becomes valid, a DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequencies to achieve frequency and phase lock with the input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL or the Fastlock bandwidth. These options are register-programmable.

The recommended mode of exit from holdover is a ramp in frequency. Just before the exit begins, the frequency difference between the output frequency while in holdover and the desired, new output frequency is measured. It is quite possible that the new output clock frequency will not be exactly the same as the holdover output frequency because the new input clock frequency might have changed and the holdover history circuit may have changed the holdover output frequency. The ramp logic calculates the difference in frequency between the holdover frequency and the new, desired output frequency. Using the user selected ramp rate, the correct ramp time is calculated. The output ramp rate is then applied for the correct amount of time so that when the ramp ends, the output frequency will be the desired new frequency. Using the ramp, the transition between the two frequencies is smooth and linear. The ramp rate can be selected to be very slow (0.2 ppm/sec), very fast (40,000 ppm/sec) or any of approximately 40 values that are in between. The loop BW values do not limit or affect the ramp rate selections and vice versa. CBPro defaults to ramped exit from holdover. Ramping is also used for ramped input clock switching. See 3.2.2 Ramped Input Switching for more information. See *AN1057: Hitless Switching using Si534x/8x Devices* for more information on Hitless and Ramped Switching with Rev. E devices.

As shown in Figure 2.1 Modes of Operation on page 13, the Holdover and Freerun modes are closely related. The device will only enter Holdover if a valid clock has been selected long enough for the holdover history to become valid, i.e. HOLD_HIST_VALID = 1. If the clock fails before the combined HOLD_HIST_LEN + HOLD_HIST_DELAY time has been met, HOLD_HIST_VALID = 0 and the device will enter Freerun mode instead. Note that the Holdover history accumulation is suspended when the input clock is removed and resumes accumulating when a valid input clock is again presented to the DSPLL. Note that when switching between input clocks with different (non-0 ppm offset) frequencies, the holdover history requires a time of 2 * HOLD_HIST_LEN + HOLD_HIST_DELAY to update the average frequency value. If a switch is initiated before this time, the average holdover frequency will be a value between the old input frequency and the new one.

Table 2.3. DSPLL Holdover Control and Status Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
Holdover Status			
HOLD_PLL	000E[7:4]	000E[5:4]	Holdover status indicator for DSPLL [D:A]. Indicates when a DSPLL is in holdover or free-run mode and is not synchronized to the input reference. The DSPLL goes into holdover only when the historical frequency data is valid, otherwise the DSPLL will be in free-run mode.
HOLD_FLG_PLL	0013[7:4]	0013[5:4]	Holdover status monitor sticky bits for DSPLL [D:A]. Sticky bits will remain asserted when an holdover event occurs until cleared. Writing a zero to a sticky bit will clear it.
HOLD_INTR_MSK_PLLA	0x0019[4]	0x0019[4]	Masks Holdover/Freerun from generating INTRb interrupt. 0: Allow Holdover/Freerun interrupt (default) 1: Mask (ignore) Holdover/Freerun for interrupt
HOLD_INTR_MSK_PLLB	0x0019[5]	0x0019[5]	
HOLD_INTR_MSK_PLLC	0x0019[6]	—	
HOLD_INTR_MSK_PLLD	0x0019[7]	—	
HOLD_HIST_VALID_PLLA	043F[1]	043F[1]	Holdover historical frequency data valid. Indicates if there is enough historical frequency data collected for valid holdover value.
HOLD_HIST_VALID_PLLB	053F[1]	053F[1]	
HOLD_HIST_VALID_PLLC	063F[1]	—	
HOLD_HIST_VALID_PLLD	0740[1]	—	
Holdover Control and Settings			
HOLD_HIST_LEN_PLLA	042E[4:0]	042E[4:0]	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds (s): Window Length = $((2^{HOLD\_HIST\text{-}LEN\_PLLx}) - 1) * 8/3 / (10^7)$
HOLD_HIST_LEN_PLLB	052E[4:0]	052E[4:0]	
HOLD_HIST_LEN_PLLC	062E[4:0]	—	
HOLD_HIST_LEN_PLLD	072F[4:0]	—	
HOLD_HIST_DELAY_PLLA	042F[4:0]	042F[4:0]	Delay Time to ignore data for historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $(2^{HOLD\_HIST\text{-}DELAY\_PLLx}) * 2/3 / (10^7)$
HOLD_HIST_DELAY_PLLB	052F[4:0]	052F[4:0]	
HOLD_HIST_DELAY_PLLC	062F[4:0]	—	
HOLD_HIST_DELAY_PLLD	0730[4:0]	—	
FORCE_HOLD_PLLA	0435[0]	0435[0]	These bits allow forcing any of the DSPLLs into holdover
FORCE_HOLD_PLLB	0535[0]	0535[0]	
FORCE_HOLD_PLLC	0635[0]	—	
FORCE_HOLD_PLLD	0736[0]	—	

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
HOLD_EXIT_BW_SEL_PLLA	042C[4]	042C[4]	Selects the exit from holdover bandwidth. Options are: 0: Exit of holdover using the fastlock bandwidth 1: Exit of holdover using the DSPLL loop bandwidth
HOLD_EXIT_BW_SEL_PLLB	052C[4]	052C[4]	
HOLD_EXIT_BW_SEL_PLLC	062C[4]	—	
HOLD_EXIT_BW_SEL_PLLD	072D[4]	—	
HOLD_RAMP_BYP_PLLA	042C[3]	042C[3]	Holdover Exit Ramp Bypass 0: Use Ramp when exiting from Holdover (default) 1: Use Holdover/Fastlock/Loop bandwidth when exiting from Holdover
HOLD_RAMP_BYP_PLLB	052C[3]	052C[3]	
HOLD_RAMP_BYP_PLLC	062C[3]	—	
HOLD_RAMP_BYP_PLLD	072D[3]	—	
HOLDEXIT_BW_SEL0_PLLA	0x049B[6]	0x049B[6]	Select the DSPLL exit bandwidth from Holdover when ramped exit is not selected (HOLD_RAMP_BYP = 1). 00: Use Fastlock bandwidth on Holdover exit 01: Use Holdover Exit bandwidth on Holdover exit (default) 10, 11: Use Normal Loop bandwidth on Holdover exit
HOLDEXIT_BW_SEL0_PLLB	0x059B[6]	0x059B[6]	
HOLDEXIT_BW_SEL0_PLLC	0x069B[6]	—	
HOLDEXIT_BW_SEL0_PLLD	0x079B[6]	—	
HOLDEXIT_BW_SEL1_PLLA	0x042C[4]	0x0x42C[4]	Select the DSPLL exit bandwidth from Holdover when ramped exit is not selected (HOLD_RAMP_BYP = 1). 00: Use Fastlock bandwidth on Holdover exit 01: Use Holdover Exit bandwidth on Holdover exit (default) 10, 11: Use Normal Loop bandwidth on Holdover exit
HOLDEXIT_BW_SEL1_PLLB	0x052C[4]	0x052C[4]	
HOLDEXIT_BW_SEL1_PLLC	0x062C[4]	—	
HOLDEXIT_BW_SEL1_PLLD	0x072D[4]	—	
RAMP_STEP_INTERVAL_PLLA	0x042C[7:5]	0x042C[7:5]	Time Interval of the frequency ramp steps when ramping between inputs or exiting holdover for each DSPLL.
RAMP_STEP_INTERVAL_PLLB	0x052C[7:5]	0x052C[7:5]	
RAMP_STEP_INTERVAL_PLLC	0x062C[7:5]	—	
RAMP_STEP_INTERVAL_PLLD	0x072D[7:5]	—	
RAMP_STEP_SIZE_PLLA	0x04A6[2:0]	0x04A6[2:0]	Size of the frequency ramp steps when ramping between inputs or exiting holdover for each DSPLL.
RAMP_STEP_SIZE_PLLB	0x05A6[2:0]	0x05A6[2:0]	
RAMP_STEP_SIZE_PLLC	0x06A6[2:0]	—	
RAMP_STEP_SIZE_PLLD	0x07A6[2:0]	—	

3. Clock Inputs (IN0, IN1, IN2, IN3/FB_IN)

The Si5381/82 supports four clock inputs that can be used to synchronize any of the DSPLLs. The inputs accept both differential and single-ended clocks. A crosspoint between the inputs and the DSPLLs allows any of the inputs to connect to any of the DSPLLs as shown in the figure below.

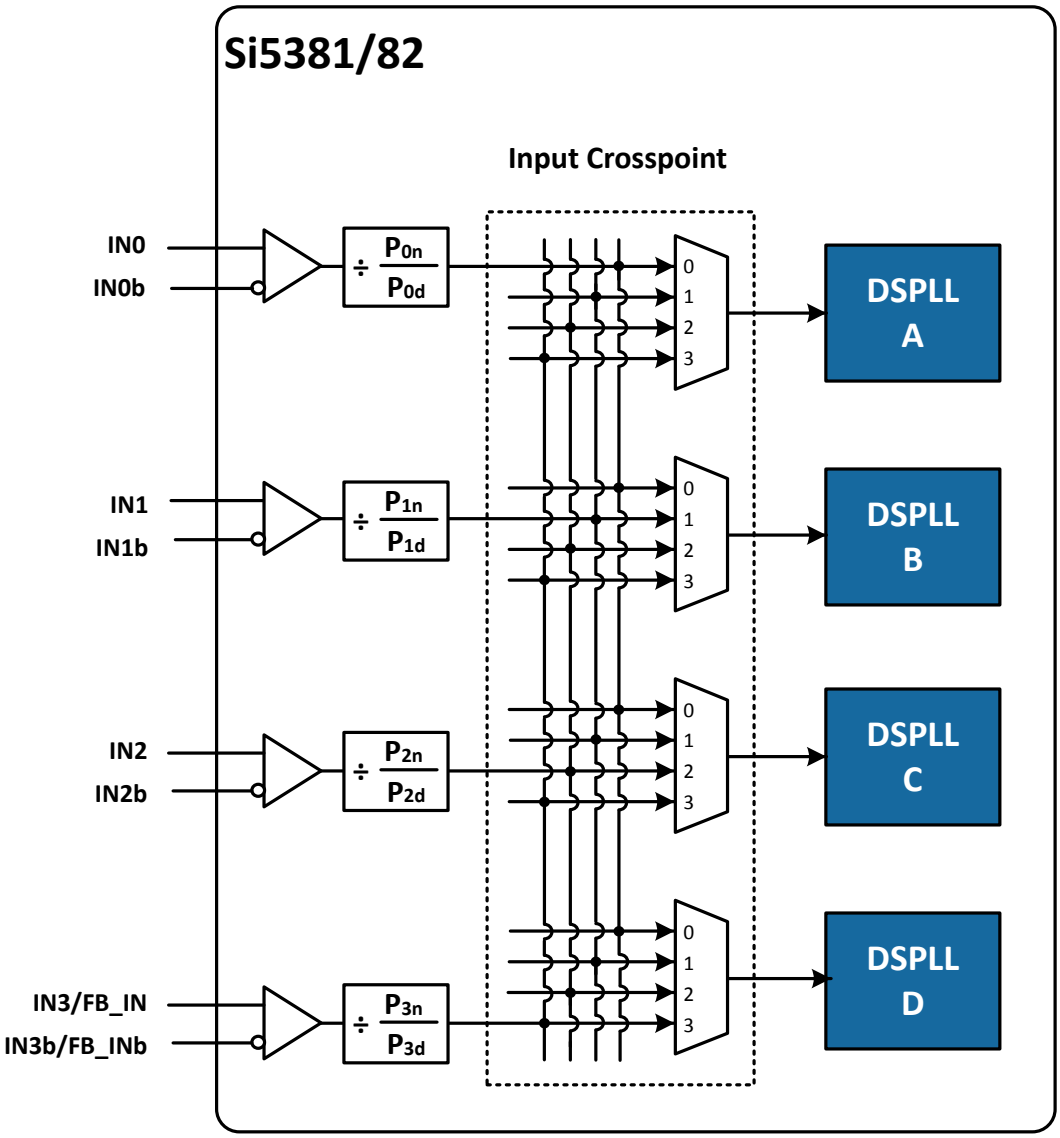


Figure 3.1. DSPLL Input Selection Crosspoint

3.1 Input Source Selection

Input source selection for each of the DSPLLs can be made manually through register control or automatically using an internal state machine. Note that all inputs to DSPLL B must come from Integer-P input dividers. ClockBuilder Pro takes this into account when generating frequency plans.

Table 3.1. Manual or Automatic Input Clock Selection Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
CLK_SWITCH_MODE_PLLA	0436[1:0]	0436[1:0]	Selects manual or automatic switching modes. Automatic mode can be Revertive or Non-revertive. Selections are the following: 00: Manual (default), 01: Automatic Non-revertive, 02: Automatic Revertive, 03: Reserved
CLK_SWITCH_MODE_PLLB	0536[1:0]	0536[1:0]	
CLK_SWITCH_MODE_PLLC	0636[1:0]	—	
CLK_SWITCH_MODE_PLLD	0737[1:0]	—	

In manual mode the input selection is made by writing to a register. If there is no clock signal on the selected input, the DSPLL will automatically enter holdover mode if the holdover history is valid or Freerun if it is not.

Table 3.2. Manual Input Select Control Register or Pin

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
IN_SEL_REGCTRL	0x052A[0]	0x052A[0]	Manual Input Select control source for DSPLL B only. 0: Pin controlled input clock selection (default) 1: IN_SEL register input clock selection

Note: IN_SEL_REGCTRL will be ignored when DSPLL B is is Zero Delay Mode. See Section 5. Zero Delay Mode for DSPLL B for more information.

Table 3.3. Manual Input Select Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
IN_SEL_PLLA	042A[2:0]	042A[2:0]	Selects the clock input used to synchronize DSPLL A, B, C, or D. Selections are: IN0, IN1, IN2, IN3, corresponding to the values 0, 1, 2, and 3. Selections 4–7 are reserved.
IN_SEL_PLLB	052A[3:1]	052A[3:1]	
IN_SEL_PLLC	062A[2:0]	—	
IN_SEL_PLLD	072B[2:0]	—	

When configured in automatic mode, the DSPLL automatically selects a valid input that has the highest configured priority. The priority arrangement is independently configurable for each DSPLL and supports revertive or non-revertive selection. All inputs are continuously monitored for loss-of-signal (LOS) and/or invalid frequency range (OOF). By default, inputs asserting either or both LOS or OOF cannot be selected as source for any DSPLL. However, these restrictions may be removed by writing to the registers described below. If there is no valid input clock, the DSP will enter either Holdover or Free Run mode depending on whether the holdover history is valid at that time or not. Note that IN3 is not available for input selection when DSPLL B is in Zero-Delay Mode.

3.1.1 Manual Input Selection

In manual mode, CLK_SWITCH_MODE=0x00.

Input switching can be done manually using the IN_SEL[1:0] device pins from the package or through registers 0x042A/0x052A/0x062A/0x072B IN_SEL_PLLx[2:1]. 0x052A[0] (IN_SEL_REG_CTRL) determines if input selection is pin selectable or register selectable. The default is pin selectable. The following table describes the input selection on the pins. Note that when Zero Delay Mode is enabled, the FB_IN pins will become the feedback input and IN3 therefore is not available as a clock input. See Section 5. Zero Delay Mode for DSPLL B for further information. If there is not a valid clock signal on the selected input, the device will automatically enter Freerun or Holdover mode.

Table 3.4. Manual Input Selection using IN_SEL[1:0] Pins

IN_SEL[1:0] PINS	DSPLL Input Source
00	IN0
01	IN1
10	IN2
11	IN3[1]

Note:

1. IN3 not available as a DSPLL source in ZDM.

3.1.2 Automatic Input Switching

In automatic mode CLK_SWITCH_MODE = 0x01 (Non-revertive) or 0x02 (Revertive).

Automatic input switching is available in addition to the manual selection described previously in 3.1.1 Manual Input Selection . In automatic mode, the switching criteria is based on input clock qualification, input priority and the revertive option. The IN_SEL0 and IN_SEL1 pins and IN_SEL register bits are not used in automatic input switching. Also, only input clocks that are valid (i.e., with no active fault indicators) can be selected by the automatic clock switching. If there are no valid input clocks available, the DSPLL will enter Holdover or Freerun mode. With Revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input will be initiated. With Non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid, an automatic switchover to the highest priority valid input will be initiated. Note that automatic input switching is not available in Zero Delay Mode. See section 5. Zero Delay Mode for DSPLL B for further information.

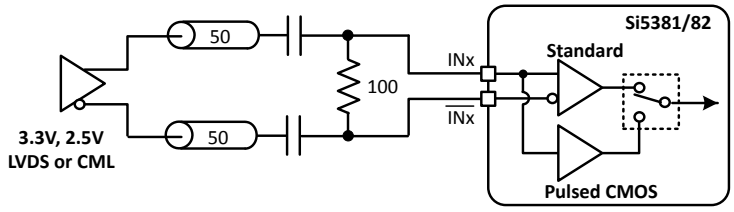
Table 3.5. Automatic Input Select Control Registers

Setting Name	Hex Address		Function
	Si5381	Si5382	
IN(3,2,1,0)_PRIORITY_PLLA	0x0438–0x0439	0x0438–0x0439	Selects the automatic selection priority for [IN3, IN2, IN1, IN0] for each DSPLL A, B, C, D. Selections are: 1st, 2nd, 3rd, 4th, or never select. Default is IN0=1st, IN1=2nd, IN2=3rd, IN3=4th.
IN(3,2,1,0)_PRIORITY_PLLB	0x0538–0x0539	0x0538–0x0539	
IN(3,2,1,0)_PRIORITY_PLLC	0x0638–0x0639	—	
IN(3,2,1,0)_PRIORITY_PLLD	0x0739–0x073A	—	
IN(3,2,1,0)_LOS_MSK_PLLA	0x0437[3:0]	0x0437[3:0]	Determines if the LOS status for [IN3, IN2, IN1, IN0] is used in determining a valid clock for the automatic input selection state machine for DSPLL A, B, C, D. Default is LOS is enabled (un-masked).
IN(3,2,1,0)_LOS_MSK_PLLB	0x0537[3:0]	0x0537[3:0]	
IN(3,2,1,0)_LOS_MSK_PLLC	0x0637[3:0]	—	
IN(3,2,1,0)_LOS_MSK_PLLD	0x0738[3:0]	—	
IN(3,2,1,0)_OOF_MSK_PLLA	0x0437[7:4]	0x0437[7:4]	Determines if the OOF status for [IN3, IN2, IN1, IN0] is used in determining a valid clock for the automatic input selection state machine for DSPLL A, B, C, D. Default is OOF enabled (un-masked).
IN(3,2,1,0)_OOF_MSK_PLLB	0x0537[7:4]	0x0537[7:4]	
IN(3,2,1,0)_OOF_MSK_PLLC	0x0637[7:4]	—	
IN(3,2,1,0)_OOF_MSK_PLLD	0x0738[7:4]	—	

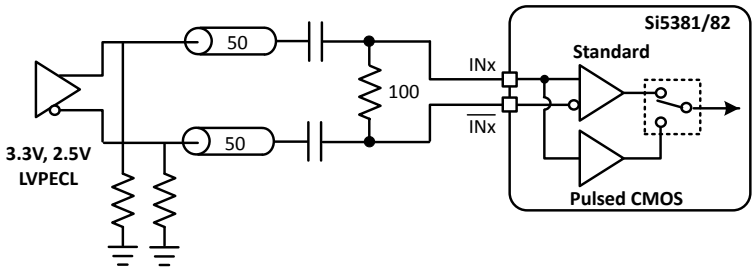
3.2 Types of Inputs

Each of the four different inputs IN0-IN3/FB_IN can be configured as standard LVDS, LVPECL, HCL, CML, and AC coupled single-ended LVCMOS formats, or as DC coupled CMOS format. The standard format inputs have a nominal 50% duty cycle, must be ac-coupled and use the “Standard” Input Buffer selection as these pins are internally dc biased to approximately 0.83 V. The pulsed CMOS input format allows pulse-based inputs, such as frame-sync and other synchronization signals, having a duty cycle much less than 50%. These pulsed CMOS signals are dc-coupled and use the “Pulsed CMOS” Input Buffer selection. In all cases, the inputs should be terminated near the device input pins as shown in the figure below. The resistor divider values given below will work with up to 1 MHz pulsed inputs. In general, following the “Standard AC Coupled Single Ended” arrangement shown below will give superior jitter performance over Pulsed CMOS.

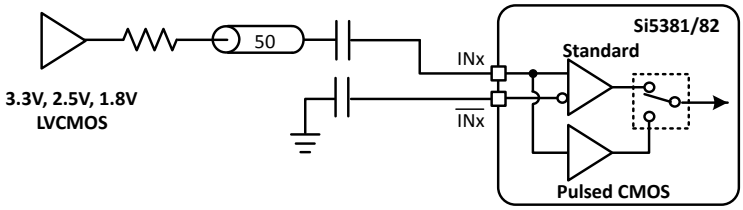
Standard AC Coupled Differential LVDS



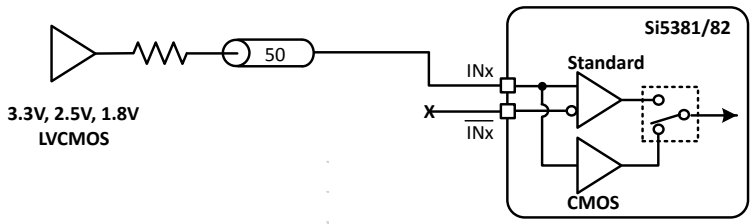
Standard AC Coupled Differential LVPECL



Standard AC Coupled Single Ended

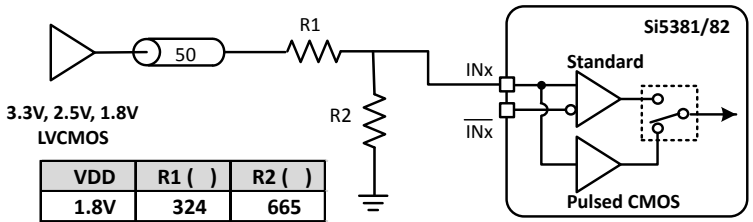


DC Coupled CMOS



IN_CMOS_USE1P8 = 1, at address 0x094F

CMOS DC Coupled Single Ended



VDD	R1 ( )	R2 ( )
1.8V	324	665
2.5V	511	475
3.3V	634	365

Figure 3.2. Input Termination for Standard and CMOS Inputs

Input clock buffers are enabled by setting the IN_EN 0x0949[3:0] bits appropriately for IN3 through IN0. Unused clock inputs may be powered down and left unconnected at the system level. For standard mode inputs, both input pins must be properly connected as shown in the figure above, including the “Standard AC Coupled Single Ended” case. In Pulsed CMOS mode, it is not necessary to connect the inverting INb input pin. To place the input buffer into Pulsed CMOS mode, the corresponding bit must be set in IN_PULSED_CMOS_EN 0x0949[7:4] for IN3 through IN0.

Table 3.6. Input Clock Configuration Registers

Register Name	Hex Address [Bit Field]	Function
IN_EN	0x0949[3:0]	Enable (or powerdown) the IN3 - IN0 input buffers. 0: Powerdown input buffer 1: Enable and Power-up input buffer
IN_PULSED_CMOS_EN	0x0949[7:4]	Select Pulsed CMOS input buffer for IN3 - IN0. 0: Standard Input Format (default) 1: Pulsed CMOS Input Format
CMOS_HI_THR	0x094F[7:4]	CMOS Clock input threshold select for inputs IN3 - IN0. 0: Low threshold (Pulsed CMOS) 1: Standard Threshold - Use with 1.8V CMOS input clocks

3.2.1 Hitless Input Switching

Hitless switching is a feature that prevents sudden phase changes from propagating to the output when switching between two clock inputs that have exactly the same frequency and a fixed phase relationship. In practice, this means that either one of the clocks must be frequency-locked to the other or that both must be frequency-locked to the same source. When hitless switching is enabled, the DSPLL absorbs the phase difference between the two input clocks during an input switch by enabling phase buildout. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. Hitless switching can be enabled on a per DSPLL basis. If a fractional P divider is used on an input, the input frequency must be 300 MHz or higher in order to ensure proper hitless switching. Note that Hitless switching is not available in Zero Delay Mode. Input switching events on DSPLL B may affect the outputs of the other A/C/D DSPLLs. See *AN1057: Hitless Switching using Si534x/8x Devices* for more information on Hitless and Ramped Switching with Rev. E devices.

Table 3.7. DSPLL Hitless Switching Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
HSW_EN_PLLA	0436[2]	0436[2]	Enable Hitless Switching. 0: Disable Hitless switching 1: Enable Hitless switching (phase buildout enabled) (default)
HSW_EN_PLLB	0536[2]	0536[2]	
HSW_EN_PLLC	0636[2]	—	
HSW_EN_PLLD	0737[2]	—	

3.2.2 Ramped Input Switching

The DSPLL has the ability to switch between two input clock frequencies that are up to ±20 ppm apart. When switching between input clocks that are not exactly the same frequency (i.e. are plesiochronous), ramped switching should be enabled to ensure a smooth transition between the two input frequencies. In this situation, it is also advisable to enable hitless switching phase buildout to minimize the input-to-output clock skew after the clock switch ramp has completed. See *AN1057: Hitless Switching using Si534x/8x Devices* for more information on Hitless and Ramped Switching with Rev. E devices.

When ramped clock switching is enabled, the DSPLL will very briefly go into holdover and then immediately exit from holdover. This means that ramped switching will behave the same as an exit from holdover. This is particularly important when switching between two input clocks that are not the same frequency because the transition between the two frequencies will be smooth and linear. Ramped switching should be turned off when switching between input clocks that are always frequency locked (i.e. are the same exact frequency). Because ramped switching avoids frequency transients and over shoot when switching between clocks that are not the same frequency, CBPro defaults to ramped clock switching. The same ramp rate settings are used for both exit from holdover and clock switching. For more information on ramped exit from holdover, see 2.5 Holdover Mode.

Table 3.8. Ramped Switching Controls

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
RAMP_SWITCH_EN_PLLA	0x04A6[3]	0x04A6[3]	Enable DSPLL Ramped Input Switching when HOLD_RAMP_BYP = 0. 0: Disable Ramped Input switching 1: Enable Ramped Input switching (Recommended)
RAMP_SWITCH_EN_PLLB	0x05A6[3]	0x05A6[3]	
RAMP_SWITCH_EN_PLLC	0x06A6[3]	—	
RAMP_SWITCH_EN_PLLD	0x07A6[3]	—	
HOLD_RAMP_BYP_PLLA	0x042C[3]	0x042C[3]	Holdover Exit Ramp Bypass 0: Use Ramp when exiting from Holdover (default) 1: Use Holdover/Fastlock/Loop bandwidth when exiting from Holdover
HOLD_RAMP_BYP_PLLB	0x052C[3]	0x052C[3]	
HOLD_RAMP_BYP_PLLC	0x062C[3]	—	
HOLD_RAMP_BYP_PLLD	0x072D[3]	—	
RAMP_STEP_INTERVAL_PLLA	0x042C[7:5]	0x042C[7:5]	Time Interval of the frequency ramp steps when ramping between inputs or exiting holdover. Set by CBPro.
RAMP_STEP_INTERVAL_PLLB	0x052C[7:5]	0x052C[7:5]	
RAMP_STEP_INTERVAL_PLLC	0x062C[7:5]	—	
RAMP_STEP_INTERVAL_PLLD	0x072D[7:5]	—	
RAMP_STEP_SIZE_PLLA	0x04A6[2:0]	0x04A6[2:0]	Size of the frequency ramp steps when ramping between inputs or exiting holdover. Set by CBPro.
RAMP_STEP_SIZE_PLLB	0x05A6[2:0]	0x05A6[2:0]	
RAMP_STEP_SIZE_PLLC	0x06A6[2:0]	—	
RAMP_STEP_SIZE_PLLD	0x07A6[2:0]	—	

3.2.3 Glitchless Input Switching

The DSPLLs have the ability to switch between two input clock frequencies that are up to ±20 ppm apart. The DSPLLs will pull-in to the new frequency at a rate determined by the DSPLLs' loop bandwidth. The DSPLLs' loop bandwidth is set using registers 0x0408 to 0x040D for DSPLL A, 0x0508 to 0x050D for DSPLL B, 0x0608 to 0x060D for DSPLL C and 0x0709 to 0x070E for DSPLL D. Note that if "Fastlock" is enabled, then the DSPLL will pull-in to the new frequency using the Fastlock Loop Bandwidth. Depending on the LOL configuration settings, the loss of lock (LOL) indicator may assert while the DSPLL is pulling-in to the new clock frequency. However, there will never be shortened "runt" output pulses generated at the output during the transition.

3.2.4 Unused Inputs

Unused inputs can be disabled and left unconnected when not in use. Register 0x0949[3:0] defaults the input clocks to being enabled. Clearing the bits for unused inputs will powerdown those inputs. For inputs which are enabled but have an inactive clock source, a weak pullup or pulldown resistor may be added to minimize noise pickup.

3.3 Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in the figure below. The XAXB reference clock is also monitored for LOS since it provides a critical reference clock for the DSPLLs. Each DSPLL also has a Loss of Lock (LOL) indicator, which is asserted when the DSPLL has lost synchronization with the selected input clock.

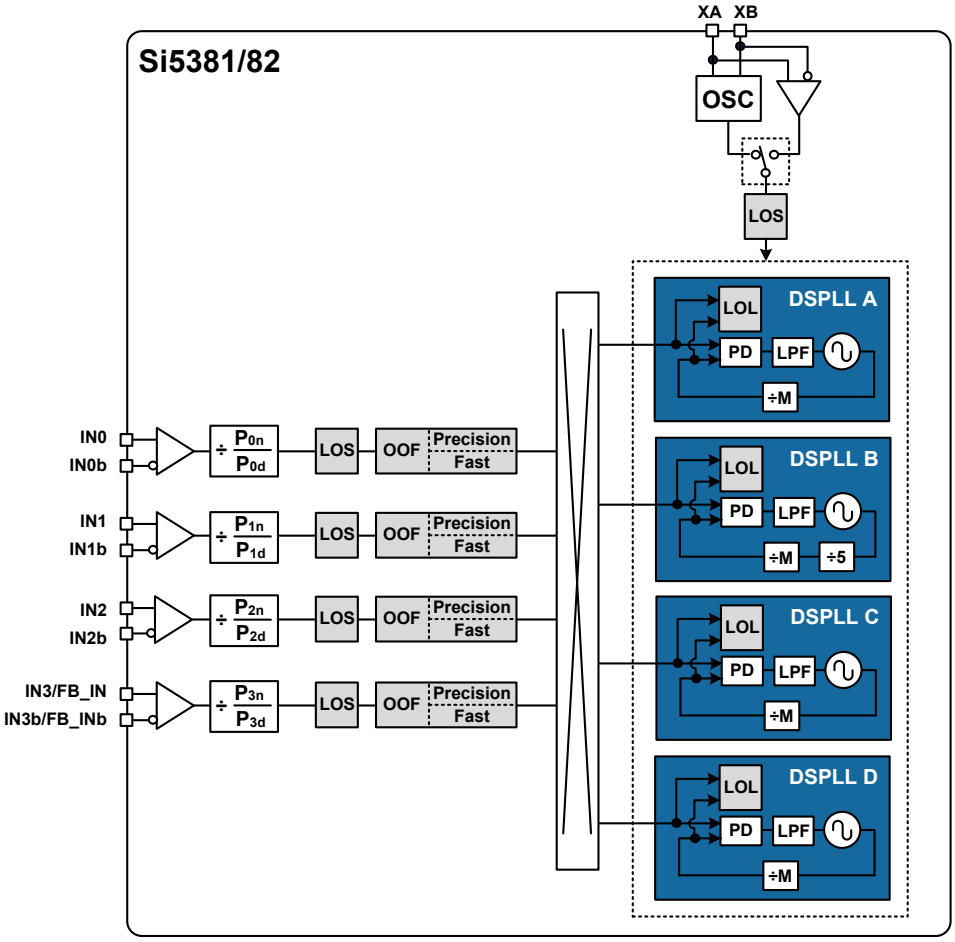


Figure 3.3. Si5381/82 Fault Monitors

3.3.1 Input LOS (Loss-of-Signal) Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity that allows missing edges or intermittent errors to be ignored. LOS sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading its status register bit. The live LOS register always displays the current LOS state. Also, there is a sticky flag register which stays asserted until cleared by the user.

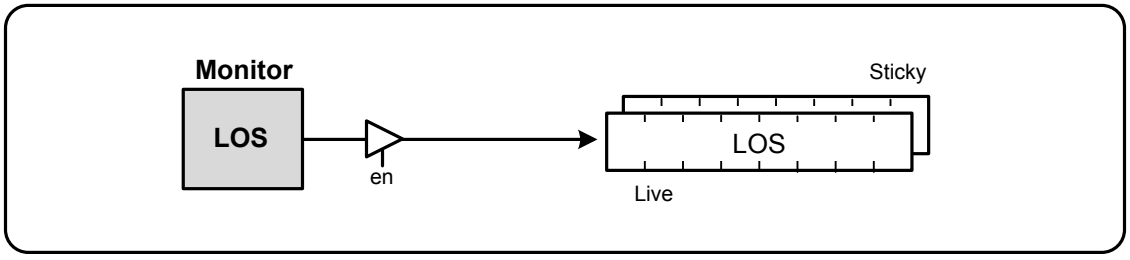


Figure 3.4. LOS Status Indicator

3.3.2 XAXB Reference Clock LOSXAXB (Loss-of-Signal) Detection

A LOS monitor is also available to ensure that the XAXB reference clock is valid. By default the output clocks are disabled when LOSXAXB is detected. This feature can be disabled such that the device will continue to produce output clocks even when LOSXAXB is detected. The table below lists the loss of signal status indicators and fault monitoring control registers.

Table 3.9. LOS Monitoring and Control Registers

Register Name	Hex Address [Bit Field]	Function
LOS Status and Controls		
LOS	0x000D[3:0]	LOS status indicators for IN3 - IN0. 0: Input signal detected or input buffer disabled or LOS disabled 1: Insufficient Input signal detected (LOS)
LOS_FLG	0x0012[3:0]	LOS indicator sticky flag bits for IN3 - IN0. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
LOS_INTR_MSK	0x0018[3:0]	Masks LOS from generating INTRb interrupt for IN3 - IN0. 0: Allow LOS interrupt (default) 1: Mask (ignore) LOS for interrupt
LOS_EN	0x002C[3:0]	LOS enable bits for IN3 - IN0. Allows disabling LOS monitors on unused inputs. 0: Disable input LOS 1: Enable input LOS
LOS_VAL_TIME	0x002D[7:0]	LOS clear validation time for IN3 - IN0. This sets the time that an input must have a valid clock before the LOS condition is cleared. 0: 2 ms, 1: 100 ms, 2: 200 ms, and 3: 1 s
LOS_TRIG_THR	0x002E[7:0]-0x0035[7:0]	Sets the LOS trigger threshold and clear sensitivity for IN3 - IN0. These values are determined by ClockBuilder Pro.
LOS_CLR_THR	0x0036[7:0]-0x003D[7:0]	
LOSXAXB Status and Controls		
LOSXAXB	0x000C[1]	LOS indicator for the XAXB reference clock 0: Reference clock signal detected 1: Reference clock signal not detected
LOSXAXB_FLG	0x0011[1]	LOSXAXB status indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
LOSXAXB_INTR_MSK	0x0017[1]	Masks LOSXAXB from generating INTRb interrupt. 0: Allow LOSXAXB interrupt (default) 1: Mask (ignore) LOSXAXB for interrupt
LOSXAXB_DIS	0x002C[4]	Enable LOS detection on the XAXB reference clock. 0: Enable LOS Detection (default). 1: Disable LOS Detection

3.3.3 Input OOF (Out-of-Frequency) Detection

Each input clock is monitored for frequency accuracy with respect to an OOF reference which it considers as its 0 ppm reference. This OOF reference can be selected as either:

- XAXB reference clock
- IN0, IN1, IN2, IN3

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky flag register bit stays asserted until cleared. Note that IN3 is only available as an OOF reference when DSPLL B is not in ZDM.

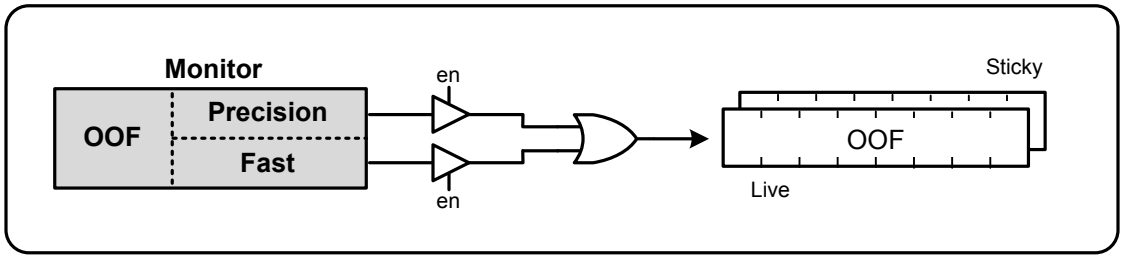


Figure 3.5. OOF Status Indicator

The Precision OOF monitor circuit measures the frequency of all input clocks to within up to ±1 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the register-programmable OOF frequency range of up to ±500 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0–IN3) as the 0 ppm OOF reference instead of the XAXB reference clock is available. These options are all register configurable.

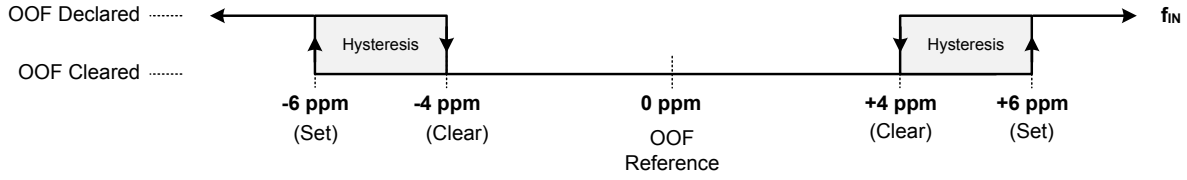


Figure 3.6. Example of Precision OOF Status Monitor Set and Clear Thresholds

The table below lists the OOF monitoring and control registers. Because the precision OOF monitor needs to provide 1 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. However, this may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF responds more quickly, and has larger thresholds.

Table 3.10. OOF Status Monitoring and Control Registers

Register Name	Hex Address [Bit Field]	Function
OOF Status and Controls		
OOF	0x000D[7:4]	OOF status indicators for IN3 - IN0. 0: Input signal detected or input buffer disabled or OOF disabled 1: Insufficient Input signal detected (OOF)
OOF_FLG	0x0012[7:4]	OOF indicator sticky flag bits for IN3 - IN0. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
OOF_INTR_MSK	0x0018[7:4]	Masks OOF from generating INTRb interrupt for IN3 - IN0. 0: Allow OOF interrupt (default) 1: Mask (ignore) OOF for interrupt
Precision OOF Controls		
OOF_EN	0x003F[3:0]	Enable Precision OOF for IN3 - IN0. 0: Disable Precision OOF 1: Enable Precision OOF
OOF_REF_SEL	0x0040[2:0]	Selects clock used for OOF as the 0 ppm reference. Selections are: XAXB, IN0, IN1, IN2, IN3. Default is XAXB. Note that IN3 may not be used when the device is in ZDM.
OOF_SET_THR	0x0046[7:0]-0x0049[7:0]	OOF Set threshold for IN3 – IN0. Range is up to ±500 ppm in steps of 1/16 ppm.
OOF_CLR_THR	0x004A[7:0]-0x004D[7:0]	OOF Clear threshold for each input. Range is up to ±500 ppm in steps of 1/16 ppm.
Fast OOF Controls		
FAST_OOF_EN	0x003F[7:4]	Enable Fast OOF for IN3 - IN0. 0: Disable Precision OOF 1: Enable Precision OOF
FAST_OOF_SET_THR	0x0051[7:0]-0x0054[7:0]	Fast OOF Set threshold for IN3 - IN0. Range is from ±1,000 ppm to ±16,000 ppm in 1000 ppm steps.
FAST_OOF_CLR_THR	0x0055[7:0]-0x0058[7:0]	OOF Clear threshold for each input. Range is from ±1,000 ppm to ±16,000 ppm in 1,000 ppm steps.

3.3.4 DSPLL Loss-of-Lock (LOL) Detection

The Loss of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock.

There are four parameters to the LOL monitor.

1. Assert to set the LOL.
   a. User sets the threshold in ppm in CBPro.
2. Fast assert to set the LOL.
   a. CBPro sets this to ~100 times the assert threshold.
   b. A very large ppm error in a short time will assert the LOL.
3. De-assert to clear the LOL.
   a. User sets the threshold in ppm in CBPro.
4. Clear delay.
   a. CBPro sets this based upon the project plan.

A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky flag register always stays asserted until cleared.

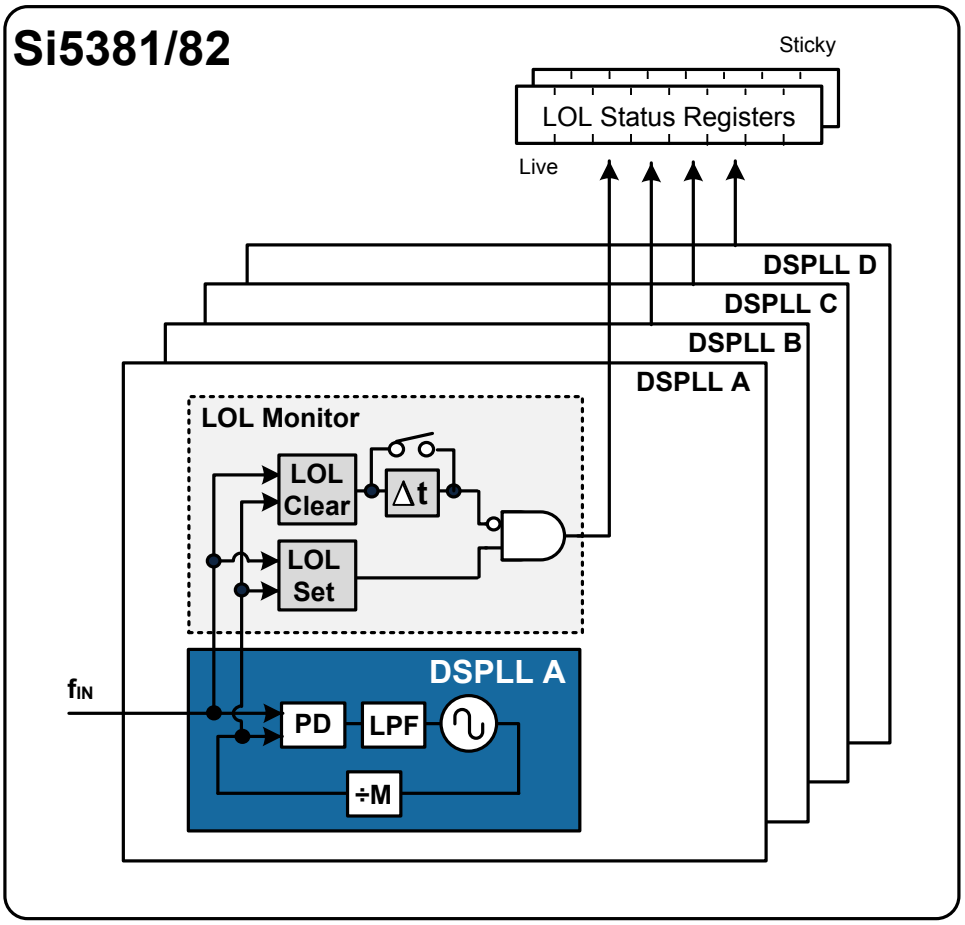


Figure 3.7. LOL Status Indicators

The LOL frequency monitor has an adjustable sensitivity which is register-configurable from ±1 ppm to ±10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 10 ppm frequency difference is shown in the figure below.

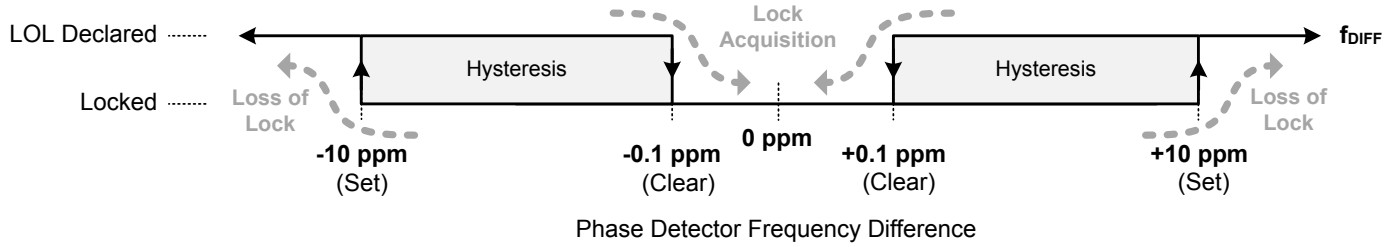


Figure 3.8. Example of LOL Set and Clear Thresholds

A timer delays clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the inpujt clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility. It is important to know that, in addition to being status bits, LOL enables Fastlock.

Table 3.11. LOL Status Monitor Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
LOL Status Indicators			
LOL_PLL	000E[3:0]	000E[1:0]	Status bit that indicates if DSPLL A, B, C, or D is locked to an input clock.
LOL_FLG_PLL	0013[3:0]	0013[1:0]	Sticky bits for LOL bits. Writing a 0 to a sticky bit will clear it.
LOL_INTR_MSK_PLL	0019[3:0]	0019[1:0]	Masks LOL from generating INTRb interrupt. 0: Allow LOL interrupt (default) 1: Mask (ignore) LOL for interrupt
LOL Fault Monitor Controls and Settings			
LOL_SET_THR_PLL	009E[7:0] - 009F[7:0]	009E[7:0]	Configures the loss of lock set thresholds for DSPLL A, B, C, D. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000, 3000, 10000. Values in ppm. Default value is 0.1 ppm.
LOL_CLR_THR_PLL	00A0[7:0] - 00A1[7:0]	00A0[7:0]	Configures the loss of lock clear thresholds for DSPLL A, B, C, D. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000, 3000, 10000. Values in ppm. Default value is 1 ppm.
LOL_CLR_DE-LAY_DIV256_PLLA	0x00A4[7:0] - 0x00A7[4:0]	0x00A4[7:0] - 0x00A7[4:0]	This is a 29-bit register that configures the delay value for the LOL Clear delay. This value de-pends on the DSPLL frequency configuration and loop bandwidth. It is calculated using the ClockBuilder Pro utility.
LOL_CLR_DE-LAY_DIV256_PLLB	0x00A9[7:0] - 0x00AC[4:0]	0x00A9[7:0] - 0x00AC[4:0]	This is a 29-bit register that configures the delay value for the LOL Clear delay. This value de-pends on the DSPLL frequency configuration and loop bandwidth. It is calculated using the ClockBuilder Pro utility.
LOL_CLR_DE-LAY_DIV256_PLLC	0x00AE[7:0] - 0x00B1[4:0]	—	This is a 29-bit register that configures the delay value for the LOL Clear delay. This value de-pends on the DSPLL frequency configuration and loop bandwidth. It is calculated using the ClockBuilder Pro utility.

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
LOL_CLR_DE-LAY_DIV256_PLLD	0x00B3[7:0] - 0x00B6[4:0]	—	This is a 29-bit register that configures the delay value for the LOL Clear delay. This value depends on the DSPLL frequency configuration and loop bandwidth. It is calculated using the ClockBuilder Pro utility.
LOL_TIMER_EN_PLL	00A2[3:0]	00A2[1:0]	Enable for the LOL Clear Timer. 0: Disable LOL clear timer 1: Enable LOL clear timer
LOL_FST_EN_PLL	0x0092[3:0]	0x0092[1:0]	Fast LOL Enable for DSPLL s D:A. Large input frequency errors will quickly assert LOL when enabled. 0: Disable Fast LOL 1: Enable Fast LOL (default)

The settings in the above table are handled by ClockBuilder Pro. Manual settings should be avoided.

3.3.5 Device Status Monitoring

In addition to the input-driven LOS, LOSXAXB, OOF, LOL, and HOLD fault monitors discussed previously, there are several additional status monitors which may be useful in determining the device operating state. While some of these indicators may seem redundant, they are either taken from different locations in the device or are active in different operating modes. These indicators can provide further insight into the operating state of the device.

Table 3.12. Device Status Monitoring and Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
SYSINCAL	0x000C[0]	0x000C[0]	Device in Calibration status indicator. 0: Normal Operation 1: Device in Calibration
LOSREF	0x000C[2]	0x000C[2]	LOS status indicator for the XAXB reference clock. 0: Reference clock signal detected 1: Reference clock signal not detected
XAXB_ERR	0x000C[3]	0x000C[3]	XAXB reference clock locking status indicator. 0: Locked to reference clock 1: Not locked to reference clock
SMBUS_TMOUT	0x000C[5]	0x000C[5]	SMB Bus Timeout Indicator. 0: SMB Bus Timeout has not occurred 1: SMB Bus Timeout Has occurred
CAL	0x000F[7:4]	0x000F[5:4]	DSPLL in Calibration status indicator for DSPLL [D:A]. 0: Normal Operation 1: DSPLL in Calibration
SYSINCAL_FLG	0x0011[0]	0x0011[0]	SYSINCAL indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
LOSREF_FLG	0x0011[2]	0x0011[2]	LOSREF indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
XAXB_ERR_FLG	0x0011[3]	0x0011[3]	XAXB_ERR indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
SMBUS_TMOUT_FLG	0x0011[5]	0x0011[5]	SMBUS_TMOUT indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.
CAL_FLG	0x0014[7:4]	0x0014[5:4]	CAL indicator sticky flag bit for DSPLL [D:A]. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.

3.3.6 INTRb Interrupt Configuration

The INTRb interrupt output pin is a convenient way to monitor a change in state of one or more status indicator flags, though direct polling may also be used to monitor device status. Each of the status indicator flags is maskable to avoid unwanted assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the unmasked status flag register bit(s) that caused the interrupt. Note that the status flag register bits cannot be cleared if the corresponding status indicator is still showing a fault.

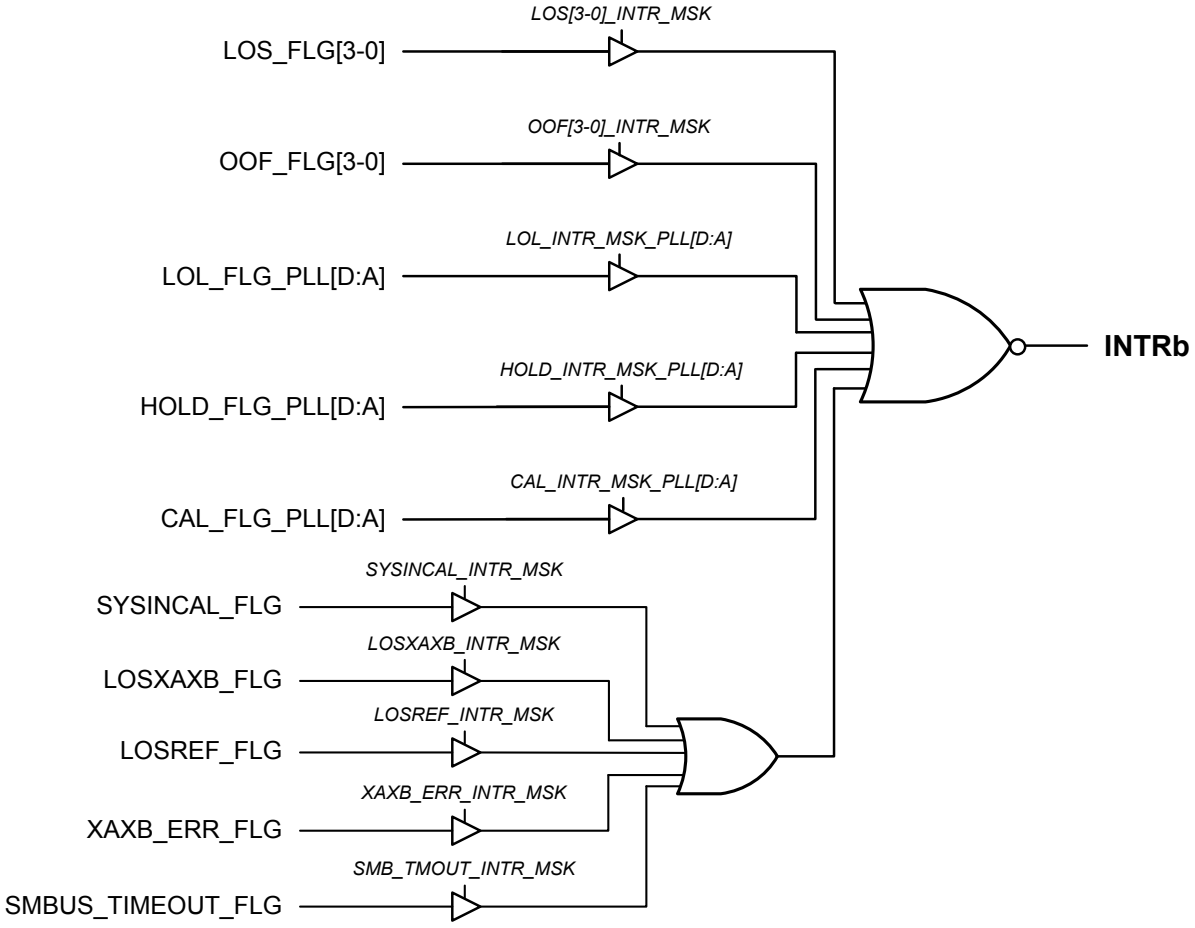


Figure 3.9. Interrupt Pin Source Masking Options

Table 3.13. INTRb Pin Interrupt Mask Registers

Register Name	Hex Address [Bit Field]	Function
LOS_INTR_MSK	0x0018[3:0]	Masks LOS from generating INTRb interrupt for IN3 - IN0. 0: Allow LOS interrupt (default) 1: Mask (ignore) LOS for interrupt
OOF_INTR_MSK	0x0018[7:4]	Masks OOF from generating INTRb interrupt for IN3 - IN0. 0: Allow OOF interrupt (default) 1: Mask (ignore) OOF for interrupt

Register Name	Hex Address [Bit Field]	Function
LOL_INTR_MSK	0x0019[3:0]	Masks LOL from generating INTRb interrupt. 0: Allow LOL interrupt (default) 1: Mask (ignore) LOL for interrupt
HOLD_INTR_MSK	0x0019[7:4]	Masks Holdover/Freerun from generating INTRb interrupt. 0: Allow Holdover/Freerun interrupt (default) 1: Mask (ignore) Holdover/Freerun for interrupt
CAL_INTR_MSK	0x001A[7:4]	Masks CAL from generating INTRb interrupt. 0: Allow CAL interrupt (default) 1: Mask (ignore) CAL for interrupt
SYSINCAL_INTR_MSK	0x0017[0]	Masks SYSINCAL from generating INTRb interrupt. 0: Allow SYSINCAL interrupt (default) 1: Mask (ignore) SYSINCAL for interrupt
LOSXAXB_INTR_MSK	0x0017[1]	Masks LOSXAXB from generating INTRb interrupt. 0: Allow LOSXAXB interrupt (default) 1: Mask (ignore) LOSXAXB for interrupt
LOSREF_INTR_MSK	0x0017[2]	Masks LOSREF from generating INTRb interrupt. 0: Allow LOSREF interrupt (default) 1: Mask (ignore) LOSREF for interrupt
XAXB_ERR_INTR_MSK	0x0017[3]	Masks XAXB_ERR from generating INTRb interrupt. 0: Allow XAXB_ERR interrupt (default) 1: Mask (ignore) XAXB_ERR for interrupt
SMB_TMOUT_INTR_MSK	0x0017[5]	Masks SMB_TMOUT from generating INTRb interrupt. 0: Allow SMB_TMOUT interrupt (default) 1: Mask (ignore) SMB_TMOUT for interrupt

4. Output Clocks

The Si5381/82 supports up to twelve differential output drivers. Each driver has a configurable voltage amplitude and common mode voltage covering a wide variety of differential signal formats, including LVPECL, LVDS, HCSL, and CML. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3V, 2.5V, or 1.8V), providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.

4.1 Output Crosspoint Switch

A crosspoint switch allows any of the output drivers to connect with any of the DSPLLs. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.

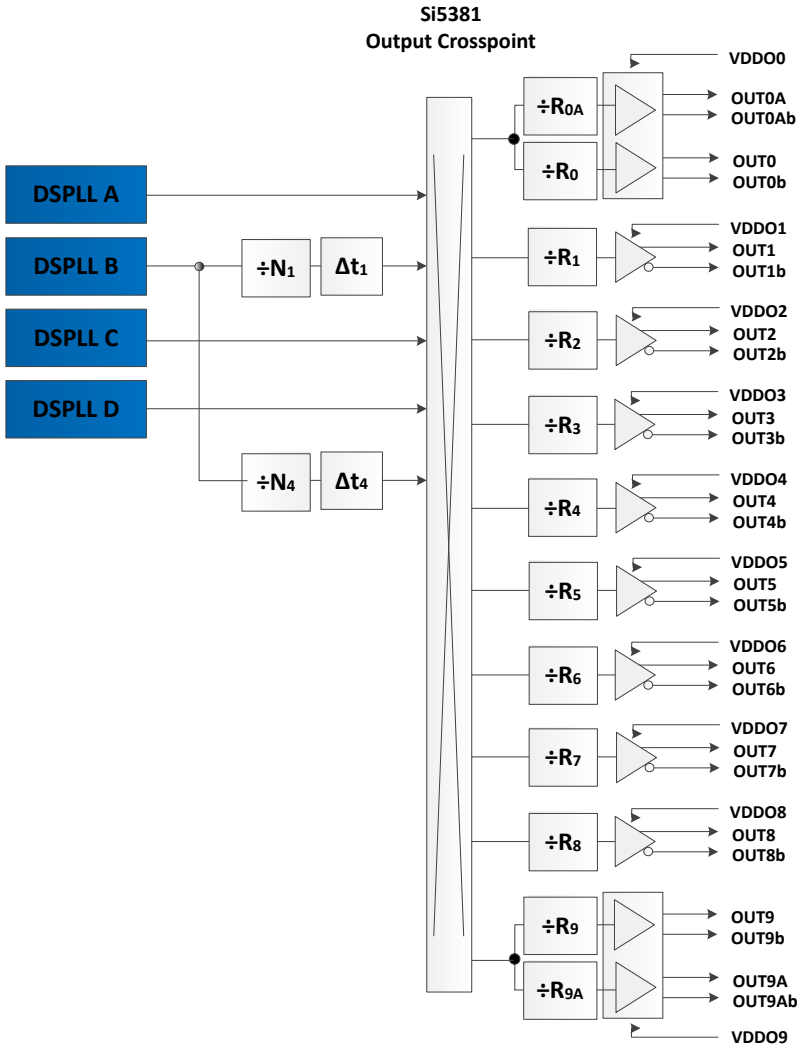


Figure 4.1. Si5381 N Divider to Output Driver Crosspoint

The following table is used to set up the routing from the N divider frequency selection to the output.

Table 4.1. Output Crosspoint Configuration Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_MUX_SEL	0x0106[2:0]	Connects the output drivers to one of the N divider sources. Selections are: 0: N0 - DSPLLA 1: N1 - DSPLL B 2: N2 - DSPLL C (Si5381), DSPLL B (Si5382) 3: N3 - DSPLL D (Si5381), DSPLL B (Si5382) 4: N4 - DSPLL B 5-7: Reserved
OUT0_MUX_SEL	0x010B[2:0]	
OUT1_MUX_SEL	0x0110[2:0]	
OUT2_MUX_SEL	0x0115[2:0]	
OUT3_MUX_SEL	0x011A[2:0]	
OUT4_MUX_SEL	0x011F[2:0]	
OUT5_MUX_SEL	0x0124[2:0]	
OUT6_MUX_SEL	0x0129[2:0]	
OUT7_MUX_SEL	0x012E[2:0]	
OUT8_MUX_SEL	0x0133[2:0]	
OUT9_MUX_SEL	0x0138[2:0]	
OUT9A_MUX_SEL	0x013D[2:0]	

4.1.1 Output R Divider Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable output phase alignment. Resetting the device using the RSTb pin or asserting the Hard Reset bit 0x001E[1] will give the same result. Also, the output R dividers can be reset by writing the SYNC register bit (0x001E[2]) high.. Soft Reset does not affect the output synchronization.

4.2 Performance Guidelines for Outputs

Whenever a number of high frequency, fast rise time, large amplitude signals are located close to one another, the laws of physics dictate that there will be some amount of crosstalk. Use of integer-related output frequencies reduces the opportunity for crosstalk as these frequencies are derived from the same output divider. The phase noise of these devices is so low that crosstalk may be detected in certain cases. Crosstalk occurs at both the device level, as well as the PCB level. It is difficult (and possibly irrelevant) to allocate the crosstalk contributions between these two sources since it can only be measured, while the device is mounted on a PCB.

In addition to following the PCB layout guidelines given in 10. XO and Device Circuit Layout Recommendations, crosstalk can be minimized by modifying the placements of the different output clock frequencies. For example, consider the following lineups of output clocks in the table below. The “Clock Placement Wizard ...” button on the “Define Output Frequencies” page of ClockBuilder Pro provides an easy way to change the frequency placements by either Manual or Automatic means.

Table 4.2. Comparison of Output Clock Frequency Placement Choices

Output	Not Recommended (Frequency MHz)	Recommended (Frequency MHz)
0A	—	155.52
0	—	—
1	100	100
2	155.52	125
3	156.25	156.25
4	122.88	—
5	125	—
6	245.76	983.04
7	983.04	491.52
8	491.52	245.76
9	—	122.98
9A	—	—

Using this example, a few guidelines are illustrated:

1. Avoid adjacent frequency values that are close in frequency. A 156.25 MHz clock should not be placed next to a 155.52 MHz clock as crosstalk will be observed at 0.73 MHz offset from each frequency. If the jitter integration bandwidth or spur range goes up to 20 MHz then keep adjacent frequencies at least 20 MHz apart.
2. Frequency values that are integer multiples of one another should be grouped together. Noting that 983.04 MHz = 2 x 491.52 MHz = 4 x 245.76 MHz = 8 x 122.88 MHz, it is okay to place each of these frequency values next to one another.
3. Unused outputs can also be placed to separate clock outputs that might otherwise show crosstalk.
4. If some outputs have tighter spur requirements while others are relatively loose, rearrange the clock outputs so that the critical outputs are the least susceptible to crosstalk.
5. Because CMOS outputs have large pk-pk swings, are single ended, and do not present a balanced load to the VDDO supplies, CMOS outputs generate much more crosstalk than differential outputs. For this reason, CMOS outputs should be avoided whenever possible. When CMOS is unavoidable, even greater care must be taken with respect to the above guidelines. For more information on these issues, see AN862 “Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems.”

4.2.1 Optimizing Output Phase Noise for Si5381/82

To obtain the best phase noise performance for RF and other demanding applications, it is important to configure the Si5381/82 devices optimally. Using DSPLL B with integer dividers for P, M, and N will provide the highest level of performance. This DSPLL and mode are optimized to support LTE, JESD204B and other integer-ratio derived frequencies. DSPLLs A, C, and D are optimized to provide maximum flexibility with fractional dividers and slightly higher phase noise.

Tips for optimizing phase noise performance, with suggestions listed most important to least important:

1. Use DSPLL B over DSPLLs A, C, or D. DSPLL B has the best inherent phase noise, while DSPLLs A, C, and D provide the most flexibility.
2. Use an Integer-N output divider. This requires the output frequency to be an even integer divisor from the VCO frequency.
3. Use Integer-P input dividers. DSPLL B requires its input dividers to be integer. DSPLLs A, C, and D may use either fractional or integer input dividers.
4. Use Integer-M feedback divider. In many cases fractional M performance is indistinguishable from integer performance. However, it is possible that there may be some cases where this measurably increases phase noise.
5. Follow the crosstalk guidelines given above in all cases. Where possible, leave an unused output between DSPLL B all-integer outputs and outputs from all other DSPLLs and even other DSPLL B N dividers. ClockBuilder Pro provides a means for manually choosing DSPLLs and DSPLL B N dividers for each output on the "Define Output Frequencies" page. Also, the "Clock Placement Wizard" allows for manual or automatic output placement to reduce the likelihood of crosstalk.

4.3 Output Signal Format

The differential output amplitude and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS, LVPECL, HCSL. For CML applications, see 15. Appendix—Custom Differential Amplitude Controls. The standard formats can be either Normal or Low-Power. Low-Power format uses less power for the same amplitude but has the drawback of slower rise/fall times. The source impedance in the Low-Power format is higher than 100 Ω. See 15. Appendix—Custom Differential Amplitude Controls for register settings to implement variable amplitude differential outputs. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3, 2.5, or 1.8 V) drivers providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs. Note also that CMOS output can create much more crosstalk than differential outputs so extra care must be taken in their pin replacement so that other clocks that need best spur performance are not on nearby pins. See *AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems* for additional information. Note that options 5 & 6 allow for only a single output pin to be active with LVCMOS signals. This reduces power consumption and also reduces crosstalk from noisy CMOS signals to other clocks. Also note that output frequencies > 1474.56 MHz are restricted to Normal Differential format with only 2.5 V and 3.3 V options allowed.

Table 4.3. Output Signal Format Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_FORMAT	0x0104[2:0]	Selects the output signal format as differential or LVCMOS mode. 0: Reserved 1: Normal Differential 2: Low-Power Differential 3: Reserved 4: LVCMOS 5: LVCMOS (OUTx pin only) 6: LVCMOS (OUTxb pin only) 7: Reserved
OUT0_FORMAT	0x0109[2:0]	
OUT1_ FORMAT	0x010E[2:0]	
OUT2_ FORMAT	0x0113[2:0]	
OUT3_ FORMAT	0x0118[2:0]	
OUT4_ FORMAT	0x011D[2:0]	
OUT5_ FORMAT	0x0122[2:0]	
OUT6_ FORMAT	0x0127[2:0]	
OUT7_ FORMAT	0x012C[2:0]	
OUT8_ FORMAT	0x0131[2:0]	
OUT9_ FORMAT	0x0136[2:0]	
OUT9A_FORMAT	0x013B[2:0]	

4.4 Output Driver Supply Select

The VDDO output driver voltage may be selected separately for each driver. The selected voltage must match the voltage supplied to that VDDO pin in the end system. VDDO pins for unused (unconnected) outputs can be left unconnected, or may be connected to a convenient 1.8 V–3.3 V system supply without increasing power dissipation.

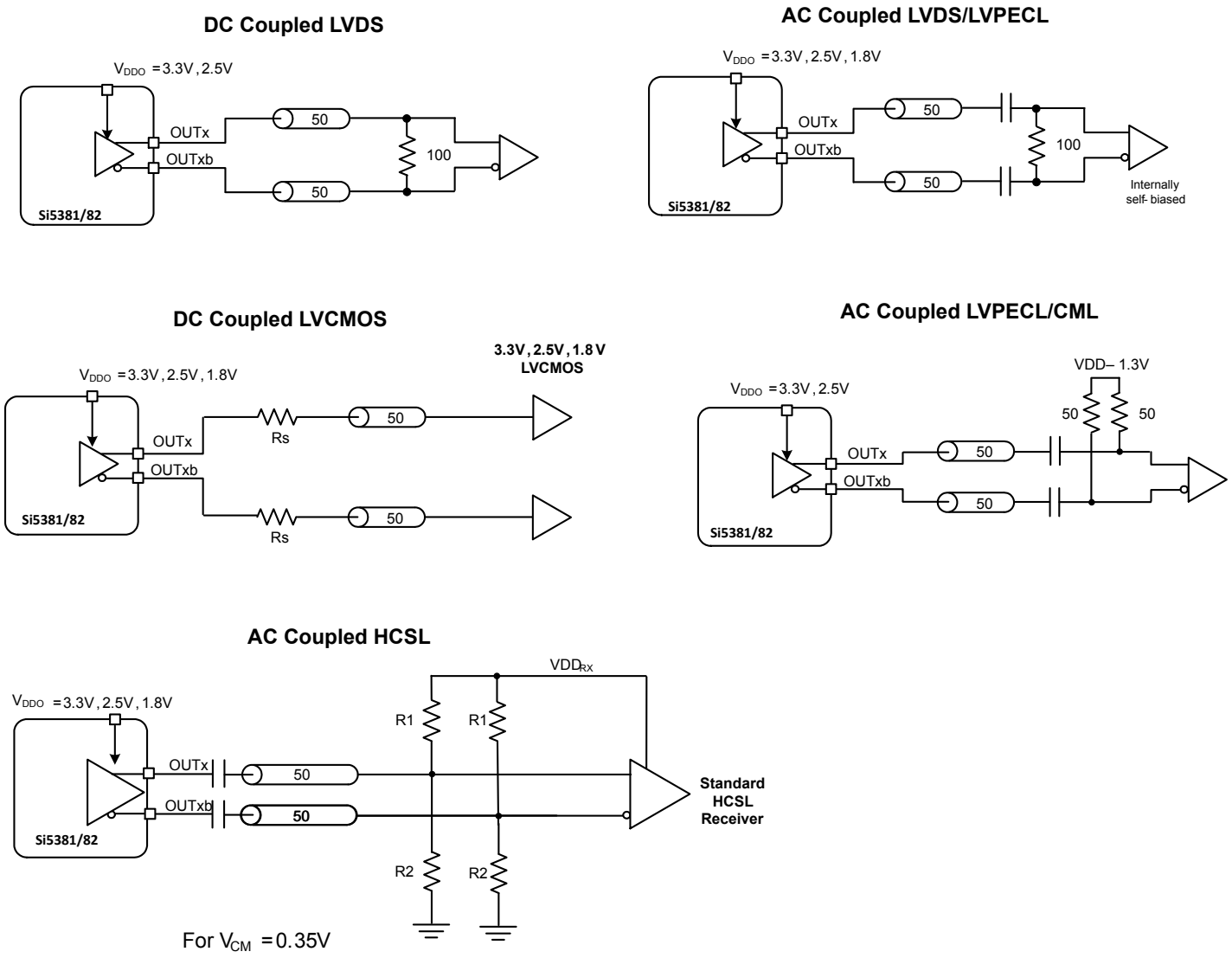
Table 4.4. Output Driver Supply Select

Register Name	Hex Address [Bit Field]	Function
OUT0A_VDD_SEL_EN	0x0106[3]	Output Driver VDD Select Enable. Set to 1 for normal operation.
OUT0A_VDD_SEL	0x0106[5:4]	Output Driver VDD select: 0: 1.8 V 1: 2.5 V 2: 3.3 V 3: Reserved
OUT0_VDD_SEL_EN	0x010B[3]	Similar to OUT0A settings.
OUT0_VDD_SEL	0x010B[5:4]	
OUT1_VDD_SEL_EN	0x0110[3]	
OUT1_VDD_SEL	0x0110[5:4]	
OUT2_VDD_SEL_EN	0x0115[3]	
OUT2_VDD_SEL	0x0115[5:4]	
OUT3_VDD_SEL_EN	0x011A[3]	
OUT3_VDD_SEL	0x011A[5:4]	
OUT4_VDD_SEL_EN	0x011F[3]	
OUT4_VDD_SEL	0x011F[5:4]	
OUT5_VDD_SEL_EN	0x0124[3]	
OUT5_VDD_SEL	0x0124[5:4]	
OUT6_VDD_SEL_EN	0x0129[3]	
OUT6_VDD_SEL	0x0129[5:4]	
OUT7_VDD_SEL_EN	0x012E[3]	
OUT7_VDD_SEL	0x012E[5:4]	
OUT8_VDD_SEL_EN	0x0133[3]	
OUT8_VDD_SEL	0x0133[5:4]	
OUT9_VDD_SEL_EN	0x0138[3]	
OUT9_VDD_SEL	0x0138[5:4]	
OUT9A_VDD_SEL_EN	0x013D[3]	
OUT9A_VDD_SEL	0x013D[5:4]	

4.5 Differential Outputs

4.5.1 Differential Output Terminations

The differential output drivers support both ac and dc-coupled terminations as shown in the following figure.



For V_{CM} =0.35V

VDD_{RX}	R1	R2
3.3V	442	56.2
2.5V	332	59
1.8V	243	63.4

Figure 4.2. Supported Differential Output Terminations

4.5.2 Differential Output Amplitude Controls

The differential amplitude of each output can be controlled with the following registers. See Table 4.7 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML on page 45 for recommended OUTx_AMPL settings for common signal formats. See 15. Appendix—Custom Differential Amplitude Controls for register settings for non-standard amplitudes.

Table 4.5. Differential Output Voltage Swing Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_AMPL	0x0105[6:4]	Sets the voltage swing for the differential output drivers for both Normal and Low-Power modes. This field only applies when OUTx_FORMAT = 1 or 2.
OUT0_AMPL	0x010A[6:4]	
OUT1_ AMPL	0x010F[6:4]	
OUT2_ AMPL	0x0114[6:4]	
OUT3_ AMPL	0x0119[6:4]	
OUT4_ AMPL	0x011E[6:4]	
OUT5_ AMPL	0x0123[6:4]	
OUT6_ AMPL	0x0128[6:4]	
OUT7_ AMPL	0x012D[6:4]	
OUT8_ AMPL	0x0132[6:4]	
OUT9_ AMPL	0x0137[6:4]	
OUT9A_ AMPL	0x013C[6:4]	

4.5.3 Differential Output Common Mode Voltage Selection

The common mode voltage (VCM) for differential output Normal and Low-Power modes is selectable depending on the supply voltage provided at the output's VDDO pin. See the table below for recommended OUTx_CM settings for common signal formats. See 15. Appendix—Custom Differential Amplitude Controls " for recommended OUTx_CM settings when using custom output amplitude.

Table 4.6. Differential Output Common Mode Voltage Selection Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_CM	0x0105[3:0]	Sets the common mode voltage for the differential output driver. This field only applies when OUTx_FORMAT = 1 or 2.
OUT0_CM	0x010A[3:0]	
OUT1_ CM	0x010F[3:0]	
OUT2_ CM	0x0114[3:0]	
OUT3_ CM	0x0119[3:0]	
OUT4_ CM	0x011E[3:0]	
OUT5_ CM	0x0123[3:0]	
OUT6_ CM	0x0128[3:0]	
OUT7_ CM	0x012D[3:0]	
OUT8_ CM	0x0132[3:0]	
OUT9_ CM	0x0137[3:0]	
OUT9A_ CM	0x013C[3:0]	

4.5.4 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML

Each differential output has four settings for control:

1. Normal or Low-Power Format
2. Amplitude (sometimes called Swing)
3. Common Mode Voltage
4. Stop High or Stop Low (See 4.7.1 Output Driver State When Disabled for details.)

The Normal mode setting includes an internal 100 Ω resistor between the OUT and OUTb pins. In Low-Power mode, this resistor is removed, resulting in a higher output impedance. The increased impedance creates larger amplitudes for the same power while reducing edge rates, which may increase jitter or phase noise. In either mode, the differential receiver must be properly terminated to the PCB trace impedance for good system signal integrity. Note that ClockBuilder Pro does not provide Low-Power mode settings. Contact Silicon Labs Technical Support for assistance with Low-Power mode use.

Amplitude controls are as described in the previous section and also in more detail in 15. Appendix—Custom Differential Amplitude Controls ". Common mode voltage selection is also described in more detail in this appendix.

Table 4.7. Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML

Standard	VDDO	Mode	OUTx_FORMAT	OUTx_CM	OUTx_AMPL
	(V)		(dec)	(dec)	(dec)
LVPECL	3.3	Normal	1	11	6
LVPECL	2.5	Normal	1	11	6
LVPECL	3.3	Low-Power	2	11	3
LVPECL	2.5	Low-Power	2	11	3
LVDS	3.3	Normal	1	3	3
LVDS	2.5	Normal	1	11	3
Sub-LVDS[1]	1.8	Normal	1	13	3
LVDS	3.3	Low-Power	2	3	1
LVDS	2.5	Low-Power	2	11	1
Sub-LVDS[1]	1.8	Low-Power	2	13	1
HCSL[2]	3.3	Low-Power	2	11	3
HCSL[2]	2.5	Low-Power	2	11	3
HCSL[2]	1.8	Low-Power	2	13	3

Notes:

1. The Sub-LVDS common mode voltage is not compliant with LVDS standards. Therefore, AC coupling the driver to an LVDS receiver is highly recommended in this case.
2. Creates HCSL compatible signals, see HCSL receiver biasing network in Figure 4.2 Supported Differential Output Terminations on page 42.

The output differential driver can also produce a wide range of CML compatible output amplitudes. See 15. Appendix—Custom Differential Amplitude Controls for additional information.

4.6 LVCMOS Outputs

4.6.1 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled as shown in the following figure.

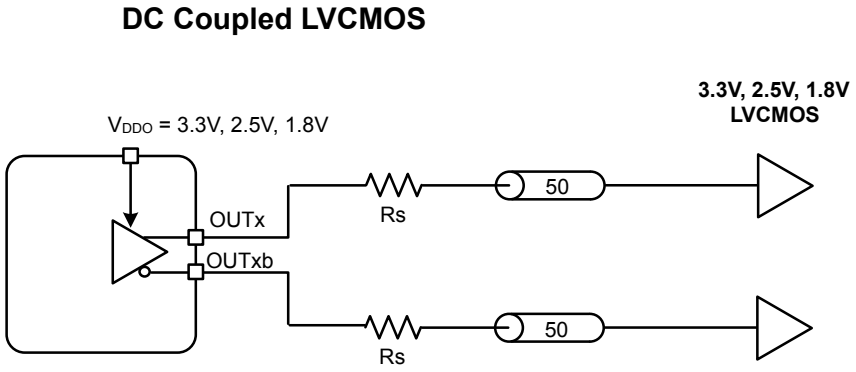


Figure 4.3. LVCMOS Output Terminations

4.6.2 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A series source termination resistor (Rs) is recommended close to the output to match the selected output impedance to the trace impedance (i.e. Rs = Trace Impedance – Zs). There are multiple programmable output impedance selections for each VDDO option as shown in the following table. Generally, the lowest impedance for a given supply voltage is preferable, since it will give the fastest edge rates.

Table 4.8. LVCMOS Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Driver Impedance (Zs)	Drive Strength (Iol/Ioh)
3.3 V	0x1	38 Ω	10 mA
	0x2	30 Ω	12 mA
	0x3[1]	22 Ω	17 mA
2.5 V	0x1	43 Ω	6 mA
	0x2	35 Ω	8 mA
	0x3[1]	24 Ω	11 mA
1.8 V	0x3[1]	31 Ω	5 mA

Note:
1. Use of the lowest impedance setting is recommended for all supply voltages.

Table 4.9. LVCMOS Drive Strength Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_CMOS_DRV	0x0104[7:6]	LVCMOS output impedance. See the table above for settings.
OUT0_CMOS_DRV	0x0109[7:6]	
OUT1_ CMOS_DRV	0x010E[7:6]	
OUT2_ CMOS_DRV	0x0113[7:6]	
OUT3_ CMOS_DRV	0x0118[7:6]	
OUT4_ CMOS_DRV	0x011D[7:6]	
OUT5_ CMOS_DRV	0x0122[7:6]	
OUT6_ CMOS_DRV	0x0127[7:6]	
OUT7_ CMOS_DRV	0x012C[7:6]	
OUT8_ CMOS_DRV	0x0131[7:6]	
OUT9_ CMOS_DRV	0x0136[7:6]	
OUT9A_ CMOS_DRV	0x013B[7:6]	

4.6.3 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers. Each output driver automatically detects the voltage on the VDDO pin to properly determine the correct output voltage.

4.6.4 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUT and OUTb). By default the clock on the OUTb pin is generated with the same polarity (in phase) with the clock on the OUT pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers. Note that these settings have no effect on the differential-mode output driver.

Table 4.10. LVCMOS Output Polarity Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_INV	0x0106[7:6]	Controls the output polarity of the OUT and OUT pins when in LVCMOS mode. Selections are shown below in the table below.
OUT0_INV	0x010B[7:6]	
OUT1_INV	0x0110[7:6]	
OUT2_INV	0x0115[7:6]	
OUT3_INV	0x011A[7:6]	
OUT4_INV	0x011F[7:6]	
OUT5_INV	0x0124[7:6]	
OUT6_INV	0x0129[7:6]	
OUT7_INV	0x012E[7:6]	
OUT8_INV	0x0133[7:6]	
OUT9_INV	0x0138[7:6]	
OUT9A_INV	0x013D[7:6]	

Table 4.11. LVCMOS Output Polarity of OUT and OUTb Pins

OUTx_INV Register Settings	OUT	OUTb	Comment
0x00	CLK	CLK	Both in phase (default)
0x01	CLK	CLKb	Complementary
0x02	CLKb	CLKb	Both Inverted
0x03	CLKb	CLK	Inverted Complementary

4.7 Output Enable/Disable

Each output driver may be individually placed in one of three operating states:

- “Enabled” state is the normal state for output clock operation. The output clock is toggling and the differential common mode voltage will be generated, if selected by the output format.
- “Disabled” state gates off clock operation and places the output into a static, user-selectable, logic state. Differential output common mode voltage is maintained, if selected by the output format, allowing a quick transition back to Enabled state operation with minimal common mode disruption.
- “Powerdown” state removes power from the output driver and leaves the output pins high-impedance. In this state, regardless of output format, the output common mode voltage is not generated and the output pin voltages are not well defined. Powerdown is recommended for unused outputs as well as startup or long-term power reduction, where differential common voltage generation restart will not introduce issues in the system. For lowest noise during operation, unused LVCMOS output pins should be AC terminated to ground with 50 Ω. See 11.1 Power Management Features for more information on powerdown.

The OEb pin provides a convenient method of enabling or disabling all of the output drivers at the same time. Holding the OEb pin low enables all of the outputs, while driving it high disables all outputs. In addition to pin control, flexible register controls described in the following sections allow further customization for each application. Note that any one disable control can disable the corresponding output(s) even if all other sources controls are enabled. See the sections below, especially 4.7.5 Output Driver Disable Source Summary , for more information on manual and automatic disable controls.

Table 4.12. Output Enable/Disable Manual Control Registers

Register Name	Hex Address [Bit Field]	Function
OUTALL_DISABLE_LOW	0x0102[0]	Enable/Disable all output drivers. If the OEb pin is held high, then all outputs will be disabled regardless of the state of this or the OUTx_OE register bits. 0: Disable All outputs (default) 1: Enable All outputs
OUT0A_OE	0x0103[1]	Enable/Disable individual outputs. Note that the OEb pin must be held low and OUTALL_DISABLE_LOW = 1 in order to enable an output. 0: Disable Output (default) 1: Enable Output
OUT0_OE	0x0108[1]	
OUT1_OE	0x010D[1]	
OUT2_OE	0x0112[1]	
OUT3_OE	0x0117[1]	
OUT4_OE	0x011C[1]	
OUT5_OE	0x0121[1]	
OUT6_OE	0x0126[1]	
OUT7_OE	0x012B[1]	
OUT8_OE	0x0130[1]	
OUT9_OE	0x0135[1]	
OUT9A_OE	0x013A[1]	

4.7.1 Output Driver State When Disabled

The disabled state of an output driver is configurable as: disable logic low or disable logic high. Note that the OUTx_DIS_STATE settings apply to Differential and LVPECL output formats.

Table 4.13. Output Driver Disable State Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_DIS_STATE	0x0104[5:4]	Determines the static state of an output driver when disabled. 0: Disable logic low 1: Disable logic high 2-3: Reserved
OUT0_DIS_STATE	0x0109[5:4]	
OUT1_ DIS_STATE	0x010E[5:4]	
OUT2_ DIS_STATE	0x0113[5:4]	
OUT3_ DIS_STATE	0x0118[5:4]	
OUT4_ DIS_STATE	0x011D[5:4]	
OUT5_ DIS_STATE	0x0122[5:4]	
OUT6_ DIS_STATE	0x0127[5:4]	
OUT7_ DIS_STATE	0x012C[5:4]	
OUT8_ DIS_STATE	0x0131[5:4]	
OUT9_ DIS_STATE	0x0136[5:4]	
OUT9A_ DIS_STATE	0x013B[5:4]	

4.7.2 Synchronous Output Enable/Disable Feature

Each of the output drivers has individually selectable synchronous or asynchronous enable/disable behavior. Output drivers with Synchronous enable/disable will wait until a clock period has completed before changing the enable state. This prevents unwanted shortened “runt” pulses from occurring. Output drivers with Asynchronous enable/disable will change the enable state immediately, without waiting for the entire clock period to complete. This selection affects both manual as well as automatic output enables and disables.

Table 4.14. Synchronous Enable/Disable Control Registers

Register Name	Hex Address [Bit Field]	Function
OUT0A_SYNC_EN	0x0104[3]	Synchronous output Enable/Disable selection. 0: Asynchronous Enable/Disable (default) 1: Synchronous Enable/Disable
OUT0_SYNC_EN	0x0109[3]	
OUT1_ SYNC_EN	0x010E[3]	
OUT2_ SYNC_EN	0x0113[3]	
OUT3_ SYNC_EN	0x0118[3]	
OUT4_ SYNC_EN	0x011D[3]	
OUT5_ SYNC_EN	0x0122[3]	
OUT6_ SYNC_EN	0x0127[3]	
OUT7_ SYNC_EN	0x012C[3]	
OUT8_ SYNC_EN	0x0131[3]	
OUT9_ SYNC_EN	0x0136[3]	
OUT9A_SYNC_EN	0x013B[3]	

4.7.3 Automatic Output Disable During LOL

By default, a DSPLL that is out of lock will generate an output clock. There is an option to disable the outputs when the DSPLL is out of lock (LOL). This option can be useful to force a downstream PLL into Holdover.

4.7.4 Automatic Output Disable During LOSXAXB

The XAXB reference clock provides a critical function for the operation of the DSPLLs. In the event of a failure the device will assert an LOSXAXB fault. By default all outputs will be disabled during assertion of the LOSXAXB fault.

Table 4.15. Output Automatic Disable on LOL and LOSXAXB Registers

Register Name	Hex Address [Bit Filed]	Function
OUT_DIS_MSK_LOL	0x0142[3:0]	Determines if the outputs are disabled during an LOL condition for DSPLL[D:A]. 0: Disable all DSPLL outputs on LOL (default) 1: Normal Operation during LOL
OUT_DIS_MSK_LOSXAXB	0x0141[7:4]	Determines if outputs are disabled during an LOSXAXB condition for DSPLL[D:A]. 0: Disable all DSPLL outputs on LOSXAXB (default) 1: All outputs remain enabled during LOSXAXB

4.7.5 Output Driver Disable Source Summary

There are a number of conditions that may cause the outputs to be automatically disabled. The user may mask out unnecessary disable sources to match system requirements. Any one of the unmasked sources may cause the output(s) to be disabled; this is more powerful, but similar in concept, to common “wired-OR” configurations. The table below summarizes the output disable sources with additional information for each source.

Table 4.16. Output Driver Summary of Disable Sources

Output Driver Disable Source	Disable Output(s) when Source...	Outputs Individually Assignable?	User Maskable?	Related Registers [bits]	Comments
OUTALL_DISABLE_LOW	Low	N	N	0x0102[0]	User Controllable
OUT0A_OE	Low	Y	N	0x0103[1]	User Controllable
OUT0_OE				0x0108[1]	
OUT1_OE				0x010D[1]	
OUT2_OE				0x0112[1]	
OUT3_OE				0x0117[1]	
OUT4_OE				0x011C[1]	
OUT5_OE				0x0121[1]	
OUT6_OE				0x0126[1]	
OUT7_OE				0x012B[1]	
OUT8_OE				0x0130[1]	
OUT9_OE				0x0135[1]	
OUT9A_OE				0x013A[1]	
OEb (pin)	High	Y	N	0x0022[1:0]	User Controllable
OE (register)	Low				
LOL_PLL[D:A]	High	N	Y	0x000D[3:0], 0x0142[3:0]	Maskable
LOSXAXB	High	N	Y	0x000C[1], 0x0141[6]	Maskable
SYSINCAL	High	N	N	0x000C[0]	Automatic, not user controllable or maskable

4.8 Output Delay Control (Δt1 – Δt4)

The Si5381 and Si5382 provide output skew delay adjustment on outputs derived from DSPLL B. Note that this function is not available for outputs derived from DSPLLs A/C/D. The Si5381 provides two independently adjustable delays on output N1 and N4 dividers. The Si5382 provides four independently adjustable delays on output N1, N2, N3, and N4 dividers.

By default all output clocks from DSPLL B are time-aligned. Each DSPLL B output N divider has an independently adjustable delay path (Δt1-Δt4) associated with it. Each of these dividers is available for applications that require deterministic output delay configuration. This is useful for PCB trace length mismatch compensation or for applications that require quadrature clock generation. Delay adjustments are bidirectional over ±8.6 ns and are programmed through registers. Fractional dividers allow a step size of 1 / F_{VCO} / 256. Integer dividers provide a step size of 1 / F_{VCO}. An example of using the Si5382 to generate two frequencies with unique configurable path delays of Δt2 and Δt3 is shown in the figure below.

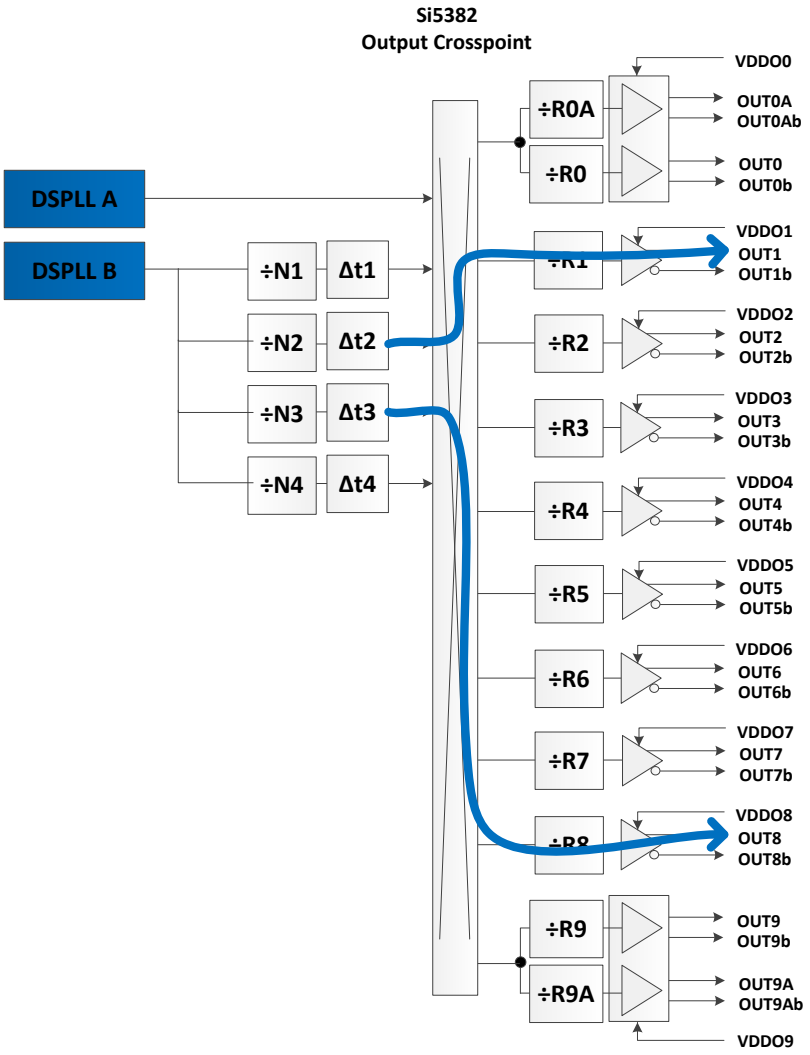


Figure 4.4. Example of Independently-Configurable Path Delays

A Soft Reset of the device, SOFT_RST_ALL (0x001C[0] = 1), is required to latch in the new delay value(s). All delay values are restored to their default values after POR, RSTb, or Hard Reset. Delay default values can be written to NVM, allowing a custom delay offset configuration at power-up or after a Hard Reset.

Table 4.17. Fractional M Divider Enable Controls

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
N1_DELAY	0x035B - 0x035C	0x035B - 0x035C	8.8-bit 2s-complement delay values. Nx_Delay values range between -128 and +127 VCO periods. t_{DLY} = Nx_DELAY / 256 × 67.8 ps, where F_{VCO} = 14.7456 GHz, $1/F_{VCO}$ = 67.8 ps
N2_DELAY (Si5382 only)	—	0x035D - 0x035E	
N3_DELAY (Si5382 only)	—	0x0359 - 0x0360	
N4_DELAY	0x0361 - 0x0362	0x0361 - 0x0362	

5. Zero Delay Mode for DSPLL B

Zero Delay Mode (ZDM) is available for DSPLL B and provides consistent minimum fixed delay between the selected input and outputs. Note that ZDM is not available for output clocks derived from DSPLL's A/C/D. ZDM is configured by opening the internal DSPLL feedback loop through software configuration and then closing the loop externally as shown in the figure below. This helps to cancel out internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. The OUT9A output and FB_IN input should be used for the external feedback connection in the Si5381/82 to minimize the overall distance and delay. In this case the pairs of pins are adjacent and polarized in such a way that no PCB vias are required to make this connection. The FB_IN input pins must be terminated and ac-coupled as shown below when Zero Delay Mode is used. A differential external feedback path connection is necessary for best performance. ClockBuilder Pro will issue a warning if this condition occurs.

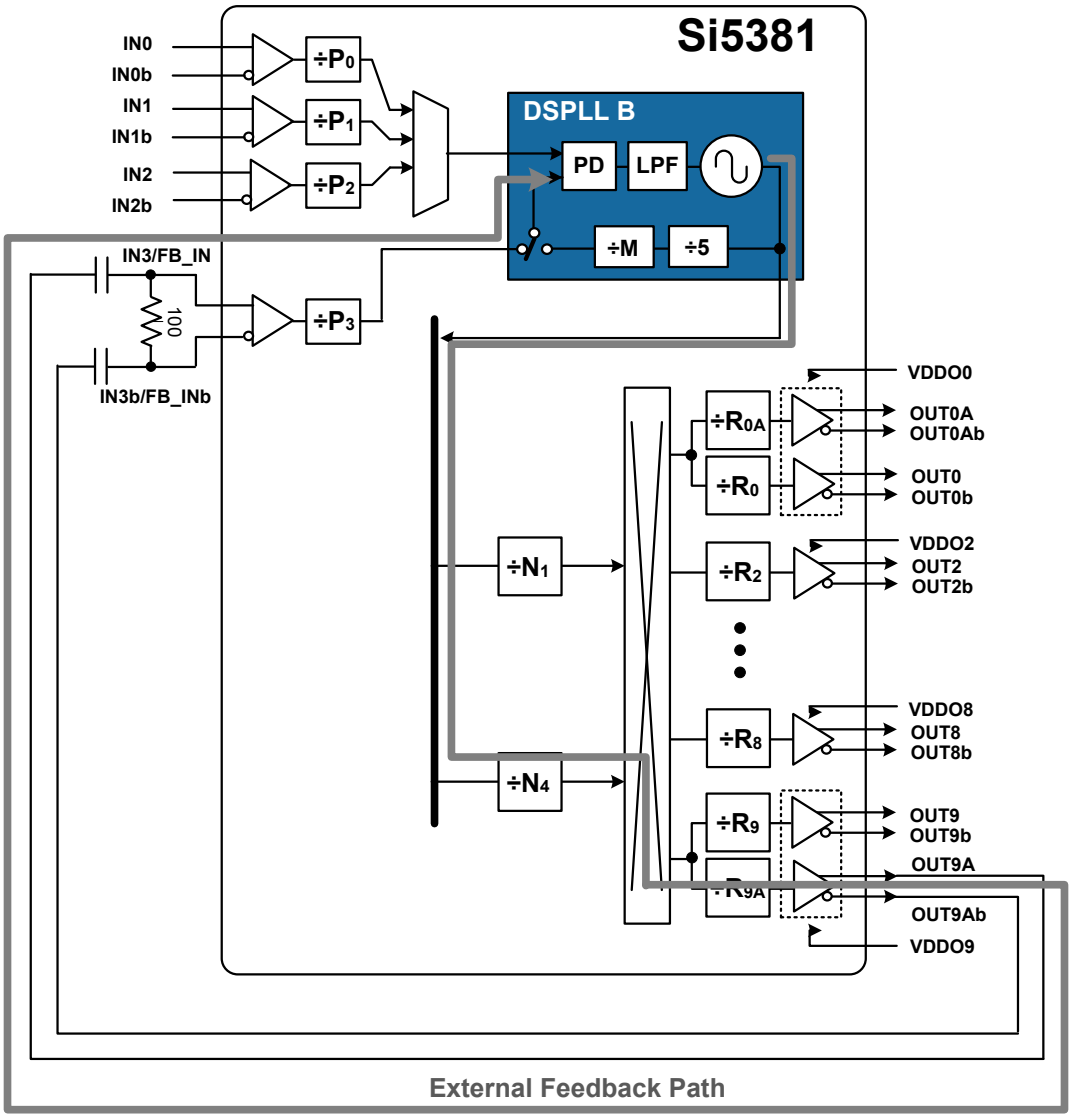


Figure 5.1. Zero Delay Mode (ZDM) Setup

To enable Zero Delay Mode (ZDM), set ZDM_EN = 1. In ZDM, the input clock source is selected manually by using either the ZDM_IN_SEL register bits or the IN_SEL1 and IN_SEL0 device input pins. IN_SEL_REGCTRL determines the choice of register or pin control to select the desired input clock. When register control is selected in ZDM, the ZDN_IN_SEL control bits determine the input to be used and the non-ZDM IN_SEL bits will be ignored. Note that in ZDM, the DSPLL will not use Hitless switching on the input clocks.

Table 5.1. Zero Delay Mode Registers

Register Name	Hex Address [Bit Field]	Function
OUTX_ALWAYS_ON	0x013F[7:0] 0x0140[3:0]	Force ZDM output always on. 0x000: Do not force output on (default) 0x800: Force OUT9A always on for ZDM
ZDM_EN	0x0487[0]	Enable ZDM operation. 0: Disable ZDM (default) 1: Enable ZDM operation
ZDM_IN_SEL	0x0487[2:1]	ZDM Manual Input Select when both ZDM_EN = 1 and IN_SEL_REGCTRL (0x052A[0]) = 1. 0: IN0 (default) 1: IN1 2: IN2 3: Reserved (IN3 already used by ZDM)
IN_SEL_REGCTRL	0x052A[0]	ZDM Manual Input Select control source for DSPLL B. 0: Pin controlled input clock selection (default) 1: ZDM_IN_SEL register input clock selection for ZDM

Note: When ZDM_EN = 1 and IN_SEL_REG_CTRL = 1, the IN_SEL pins and register bits have no effect.

Table 5.2. Input Clock Selection in Zero Delay Mode

Register Name	Hex Address [Bit Field]	Function
ZDM_EN		Input Clock Selection Governed by:
IN_SEL_REGCTRL		0 0 IN_SEL[1:0] Pins 0 1 IN_SEL Register 1 0 IN_SEL[1:0] Pins (ZDM) 1 1 ZDM_IN_SEL Register (ZDM)

6. Digitally Controlled Oscillator (DCO) Mode

DSPLLs A, C, and D support a DCO mode where their output frequencies are adjustable in pre-defined steps given by frequency step words (FSTEPW). The frequency adjustments are controlled through the serial interface or by pin control using frequency increments (FINC) or decrements (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. The DCO mode is available when the DSPLL is operating in locked mode. Note that the maximum FINC/FDEC update rate is 1 MHz. Each DSPLL being used in DCO mode should have fractional M division enabled by setting the appropriate M_FRAC_EN_PLLx=0x3B for proper operation. See AN909: DCO Application with the Si5347/46 for related information. Note that DCO is not available for Si5381/82 DSPLL B, or for any DSPLL in Freerun mode.

Table 6.1. Fractional M Divider Enable Controls for DCO

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
M_FRAC_EN_PLLA	0x0421[7:0]	0x0421[7:0]	DSPLL feedback M divider fractional enable. 0x2B: Integer-only division 0x3B:Fractional (or Integer) division Required for DCO operation.
M_FRAC_EN_PLLC	0x0621[7:0]	—	
M_FRAC_EN_PLLD	0x0722[7:0]	—	

6.1 Frequency Increment/Decrement Using the Serial Interface

Controlling the DSPLL frequency through the serial interface is available on both the Si5381 and Si5382. This can be performed by asserting the FINC or FDEC bits to activate the frequency range defined by the frequency step word. A set of mask bits selects the DSPLL(s) that is affected by the frequency change. Note that both the FINC and FDEC register bits are rising-edge-triggered and self-clearing.

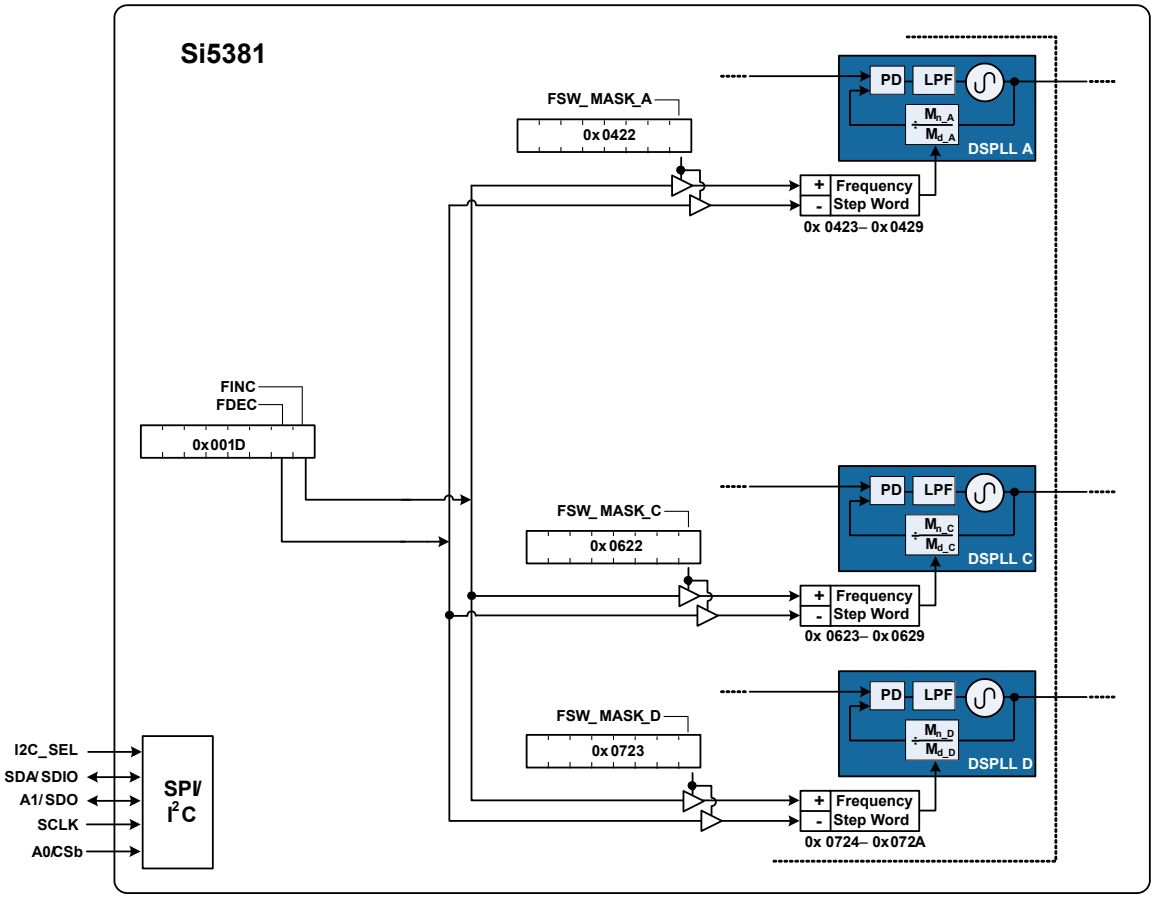


Figure 6.1. Controlling the DCO Mode Using the Serial Interface

Table 6.2. Frequency Increment/Decrement Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5381	Si5382	
FINC	001D[0]	001D[0]	Asserting this bit will increase the DSPLL output frequency by the frequency step word.
FDEC	001D[1]	001D[2]	Asserting this bit will decrease the DSPLL output frequency by the frequency step word.
M_FSTEPW_PLLA	0423[7:0]-0429[7:0]	0423[7:0]-0429[7:0]	This is a 56-bit frequency step word for DSPLL A, C, and D. FSTEPW will be added to or subtracted from the DSPLL output frequency during assertion of the FINC/FDEC bits or pins. FSTEPW is calculated based on the frequency configuration and is easily calculated using ClockBuilder Pro utility.
M_FSTEPW_PLLC	0623[7:0]-0629[7:0]	—	
M_FSTEPW_PLLD	0724[7:0]-072A[7:0]	—	
M_FSTEP_MSK_PLLA	0422[0]	0422[0]	This mask bit determines if a FINC or FDEC affects DSPLL A, C, D. 0: Enable FINC/FDEC to increment/decrement the FSTEPW to the DSPLL. 1: Ignores FINC/FDEC.
M_FSTEP_MSK_PLLC	0622[0]	—	
M_FSTEP_MSK_PLLD	0723[0]	—	

7. Serial Interface

Configuration and operation of the Si5381/82 is controlled by reading and writing registers using the I²C or SPI interface. The I²C_SEL pin selects I²C or SPI operation. The Si5381/82 supports communication with a 3.3 V or 1.8 V host by setting the IO_VDD_SEL (0x0943[0]) configuration bit. The SPI interface supports both 4-wire or 3-wire modes by setting the SPI_3WIRE (0x002B[3]) configuration bit. See the figure below for supported modes of operation and settings. All digital I/O pins are 3.3 V-tolerant, even when operating at 1.8 V. Additionally, the pins with internal pull-ups, I2C_SEL and A0/CSb are pulled-up to 3.3 V through a high impedance pull-up, regardless of IO_VDD_SEL setting.

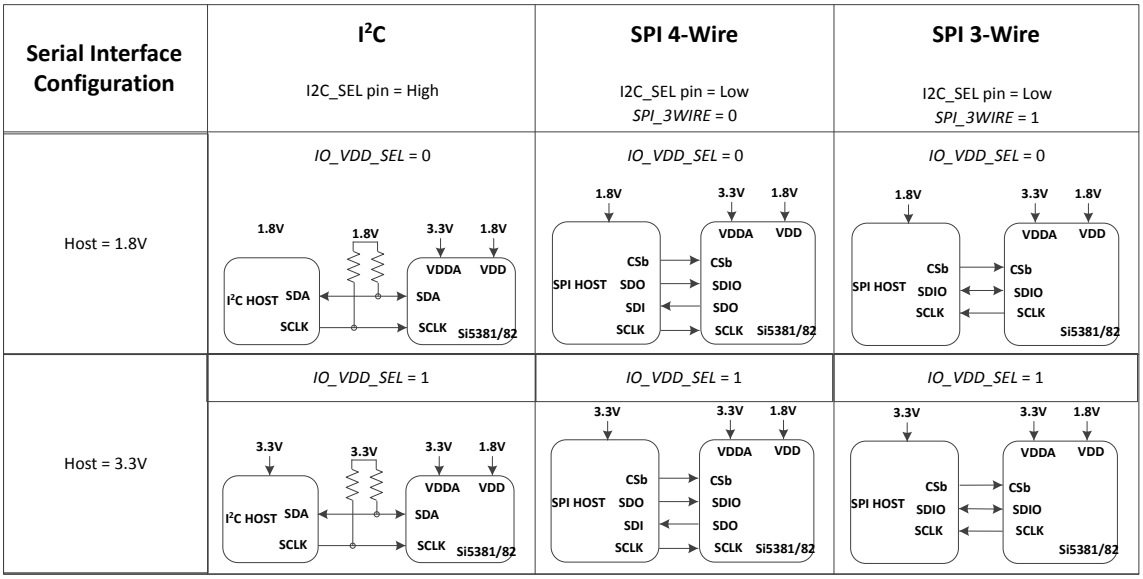


Figure 7.1. I2C/SPI Device Connectivity Configurations

In some cases it is not known prior to the design, what the serial interface type and I/O voltage will be. Setting the device to 1.8 V (IO_VDD_SEL = 0) digital I/O in the NVM allows the host to reliably write the device, regardless of its operating voltage. Once the serial interface type has been chosen using the I²C_SEL pin, the device may be written successfully regardless of the host interface type. This is true for both 3-wire and 4-wire SPI modes as well as I²C. The SPI serial data is written to the same SDA/SDIO input pin in all cases. At this point, the device can be configured to adjust IO_VDD_SEL for optimum 3.3 V operation and to select SPI_3WIRE between 3-/4-wire SPI modes. These mode changes are made immediately and no delays or wait times are needed for subsequent serial interface operations, including read operations.

Note that the registers are organized into multiple pages to allow a larger register set, given the limitations of the I²C/SPI interface standards. First, the correct page must be selected with the initial write. Then the register location within that page can be read/written. See AN926: Reading and Writing Registers with SPI and I²C for Si534x/8x Devices for more information on register paging.

If neither serial interface is used, the SDA/SDIO, A1/SDO, and SCLK pins must be pulled either high or low externally since they are not pulled internally. I²C_SEL and A0/CSb have internal pull-ups and may be left unconnected in this case. Note that the Si5381/82 is not I²C failsafe upon loss of power. Applications that require failsafe operation should isolate the device from a shared I²C bus.

The following table lists register settings of interest for the I²C/SPI serial interface operation.

Table 7.1. I2C/SPI Configuration Registers

Register Name	Hex Address [Bit Field]	Function
IO_VDD_SEL	0x0943[0]	Select digital I/O operating voltage. 0: 1.8 V digital I/O connections (default) 1: 3.3 V digital I/O connections
SPI_3WIRE	0x002B[3]	Selects operating mode for SPI interface: 0: 4-wire SPI (default) 1: 3-wire SPI
I2C_ADDR	0x000B[6:0]	7-bit I2C Address. See 7.1 I²C Interface for more information.

7.1 I²C Interface

When in I²C mode, the serial interface operates in slave mode with 7-bit addressing and operates in either Standard-Mode (100 kbps) or Fast-Mode (400 kbps) while supporting burst data transfer with auto address increments. The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in the figure below. Both the SDA and SCL pins must be connected to a supply via an external pull-up (4.7 kΩ) as recommended by the I2C specification. Two address select pins, A1 and A0, are provided, allowing up to four Si5381 devices to communicate on the same bus. This also allows four choices in the I²C address for systems that may have other overlapping addresses for other I²C devices.

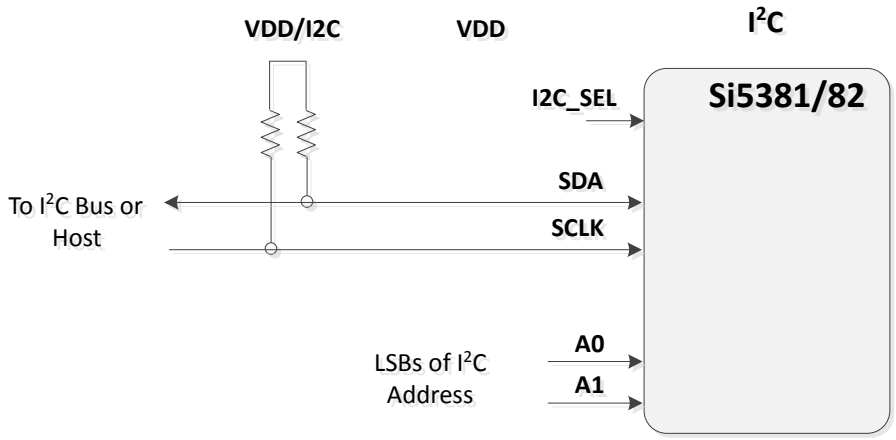


Figure 7.2. I2C Configuration

The 7-bit I²C slave device address of the Si5381/82 consists of a 5-bit fixed address plus two bit determined by the voltages on the A1 and A0 input pins, as shown in the figure below.

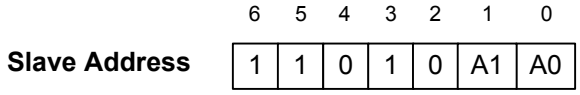


Figure 7.3. 7-bit I2C Slave Address Bit-Configuration

The I²C bus supports SDA timeout for compatibility with SMB Bus interfaces. The error indicator and flag are listed in the registers listed in the table below. See 3.3 Fault Monitoring for more information.

Table 7.2. SMB Bus Timeout Error Registers

Register Name	Hex Address [Bit Field]	Function
SMB_TMOUT	0x000C[5]	SMB Bus Timeout Indicator. 0: SMB Bus Timeout has Not occurred 1: SMB Bus Timeout Has occurred
SMB_TMOUT_FLG	0x0011[5]	SMB_TMOUT indicator sticky flag bit. Remains asserted after the indicator bit shows a fault until cleared by the user. Writing a 0 to the flag bit will clear it if the indicator bit is no longer asserted.

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in the figure below. A write burst operation is also shown where subsequent data words are written using to an auto-incremented address.

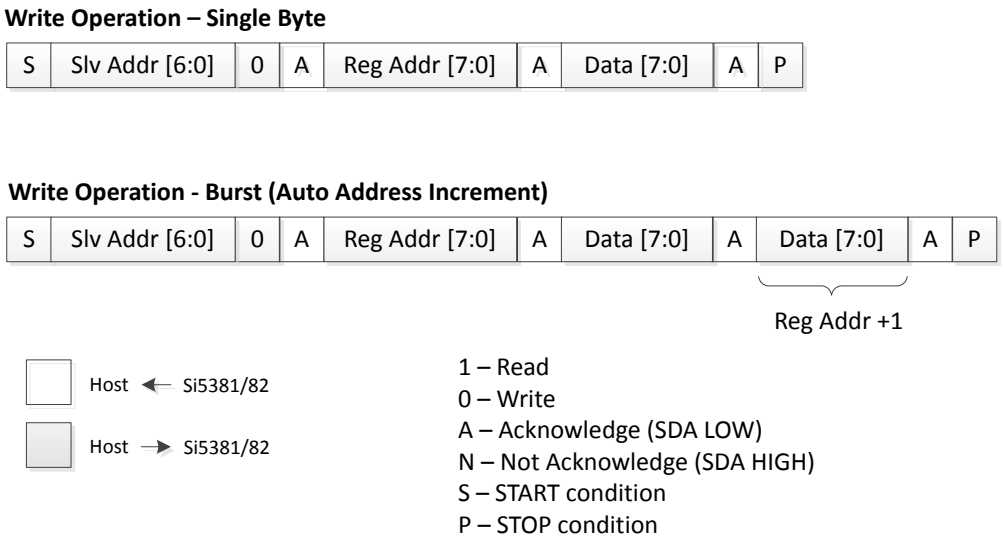


Figure 7.4. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in the following figure.

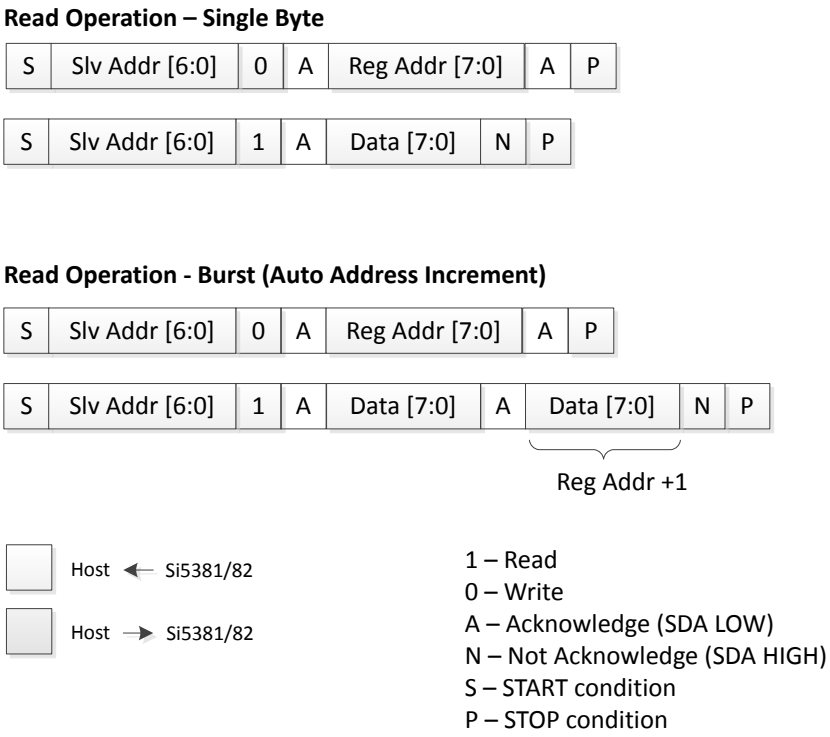


Figure 7.5. I²C Read Operation

7.2 SPI Interface

When in SPI mode, the serial interface operates in 4-wire or 3-wire depending on the state of the SPI_3WIRE configuration bit, 0x000B[3]. The 4-wire interface consists of a clock input (SCLK), a chip select input (CSb), serial data input (SDI), and serial data output (SDO). The 3-wire interface combines the SDI and SDO signals into a single bidirectional data pin (SDIO). Both 4-wire and 3-wire interface connections are shown in the following figure.

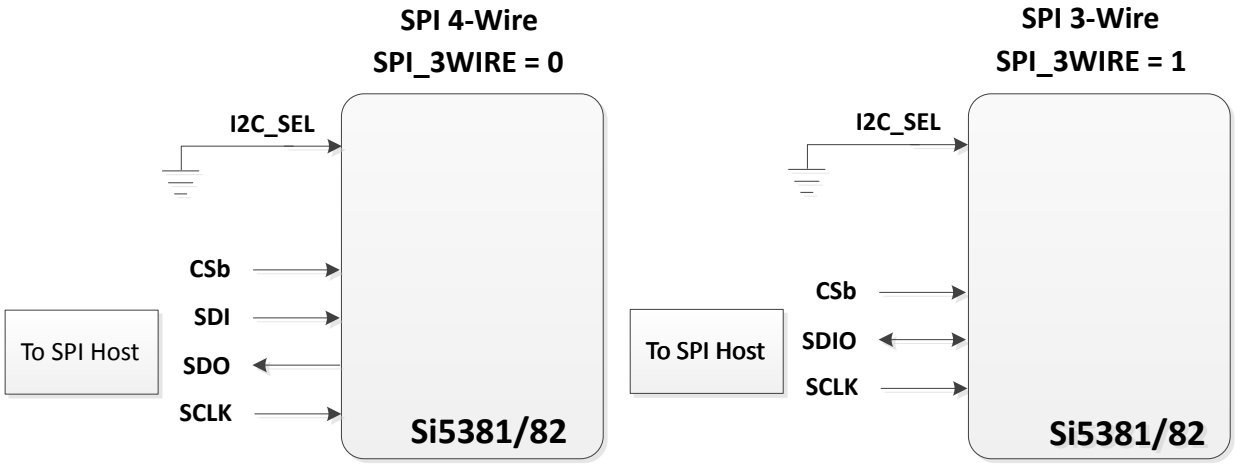


Figure 7.6. SPI Interface Connections

Table 7.3. SPI Command Formats

Instruction	Ist Byte[1]	2nd Byte	3rd Byte	Nth Byte[2,3]
Set Address	000x xxxx	8-bit Address	—	—
Write Data	010x xxxx	8-bit Data	—	—
Read Data	100x xxxx	8-bit Data	—	—
Write Data + Address Increment	011x xxxx	8-bit Data	—	—
Read Data + Address Increment	101x xxxx	8-bit Data	—	—
Burst Write Data	1110 0000	8-bit Address	8-bit Data	8-bit Data

Note:

1. X = don't care (1 or 0)
2. The Burst Write Command is terminated by de-asserting CSb (CSb = high)
3. There is no limit to the number of data bytes that follow the Burst Write Command, but the address will wrap around to zero in the byte after address 255 is written.

Writing or reading data consist of sending a “Set Address” command followed by a “Write Data” or “Read Data” command. The 'Write Data + Address Increment' or “Read Data + Address Increment” commands are available for cases where multiple byte operations in sequential address locations is necessary. The “Burst Write Data” instruction provides a compact command format for writing data since it uses a single instruction to define starting address and subsequent data bytes. The first figure below shows an example of writing three bytes of data using the write commands. This demonstrates that the “Write Burst Data” command is the most efficient method for writing data to sequential address locations. Figure 7.8 Example of Reading Three Data Bytes Using the SPI Read Commands on page 65 provides a similar comparison for reading data with the read commands. Note that there is no burst read, only read increment.

'Set Address' and 'Write Data'

'Set Addr'	Addr [7:0]	'Write Data'	Data [7:0]
'Set Addr'	Addr [7:0]	'Write Data'	Data [7:0]
'Set Addr'	Addr [7:0]	'Write Data'	Data [7:0]

'Set Address' and 'Write Data + Address Increment'

'Set Addr'	Addr [7:0]	'Write Data + Addr Inc'	Data [7:0]
'Write Data + Addr Inc'	Data [7:0]		
'Write Data + Addr Inc'	Data [7:0]		

'Burst Write Data'

'Burst Write Data'	Addr [7:0]	Data [7:0]	Data [7:0]	Data [7:0]

Figure 7.7. Example Writing Three Data Bytes Using the SPI Write Commands

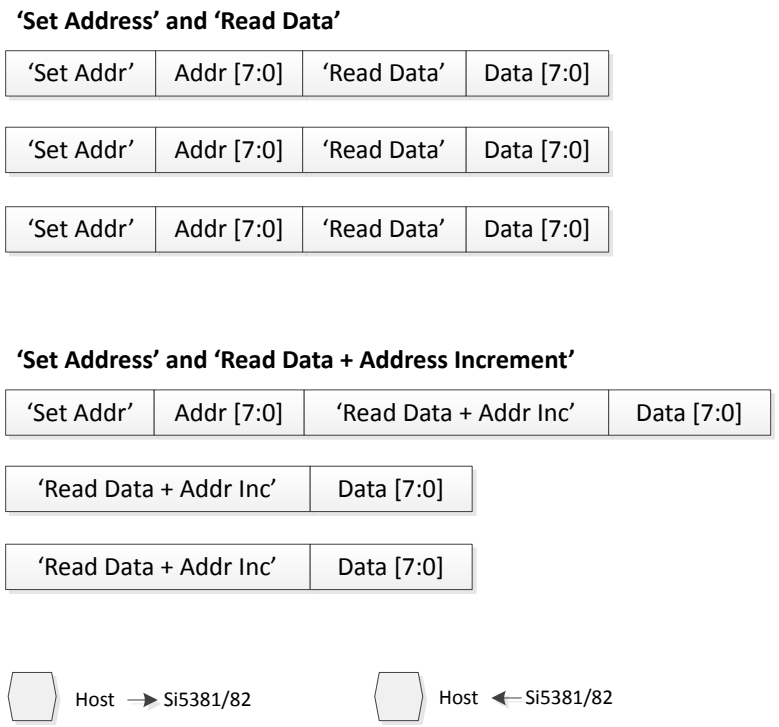


Figure 7.8. Example of Reading Three Data Bytes Using the SPI Read Commands

The timing diagrams for the SPI commands are shown in the following figures.

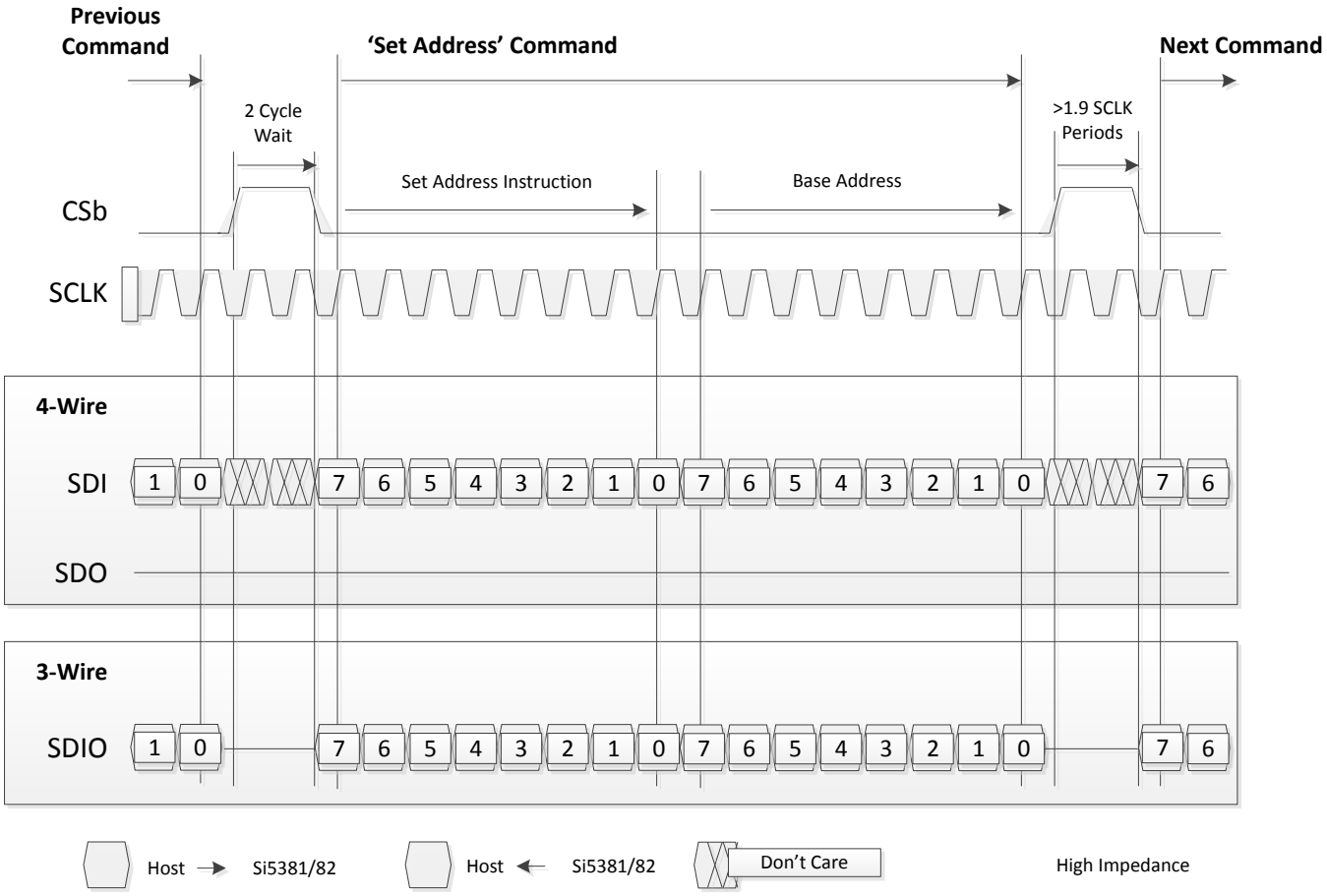


Figure 7.9. SPI "Set Address" Command Timing

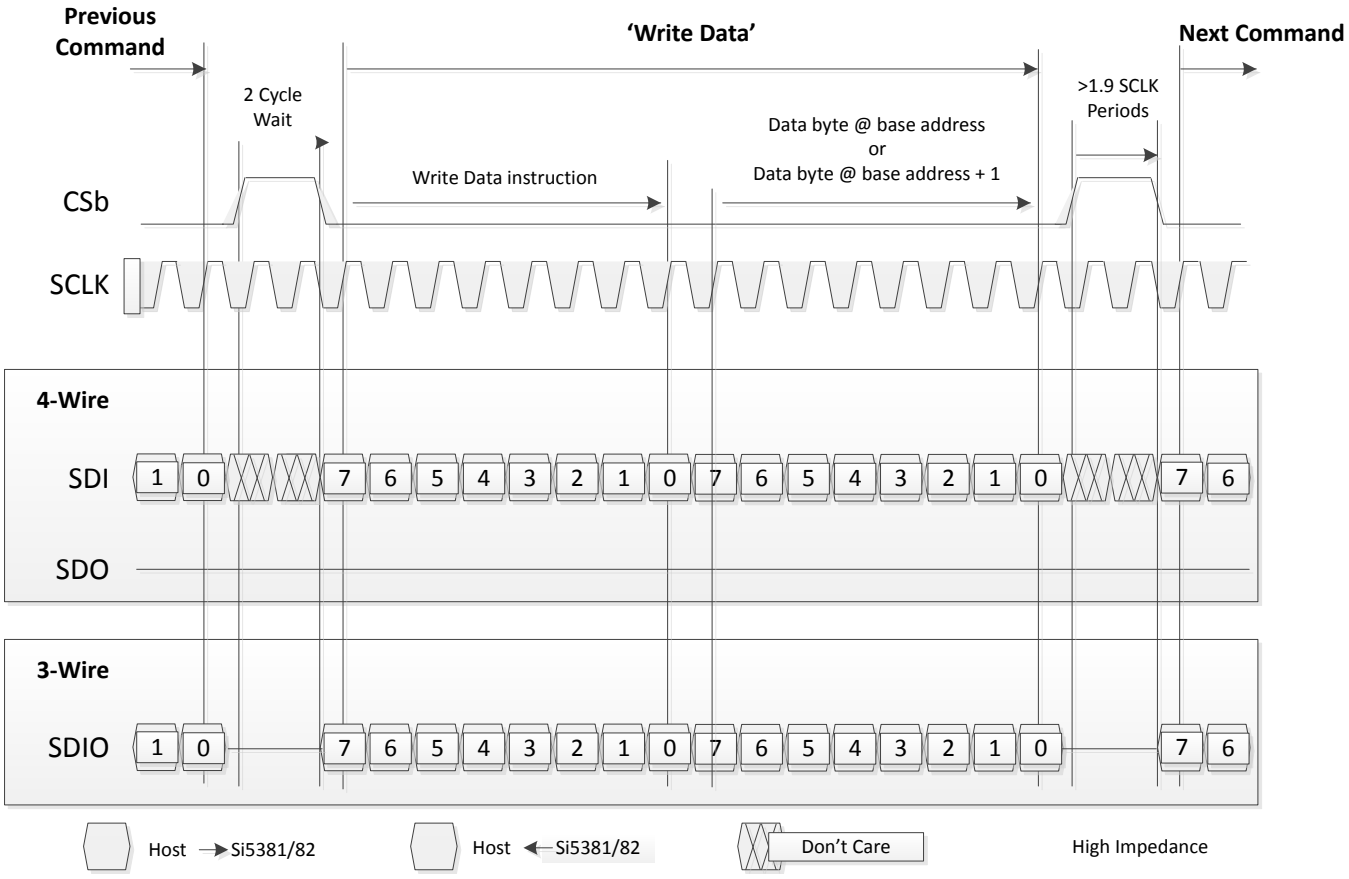


Figure 7.10. SPI "Write Data" and "Write Data + Address Increment" Instruction Timing

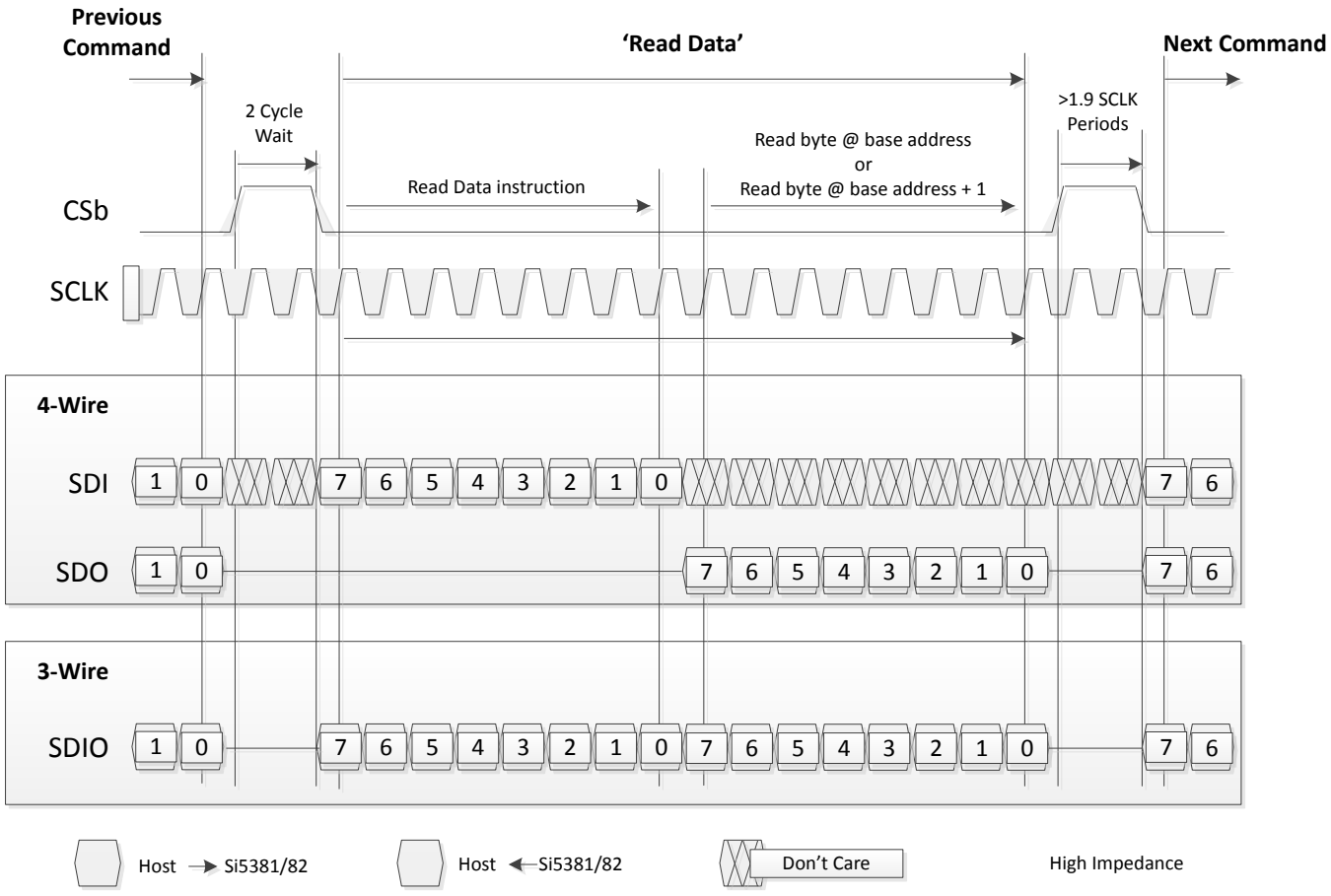


Figure 7.11. SPI "Read Data" and "Read Data + Address Increment" Instruction Timing

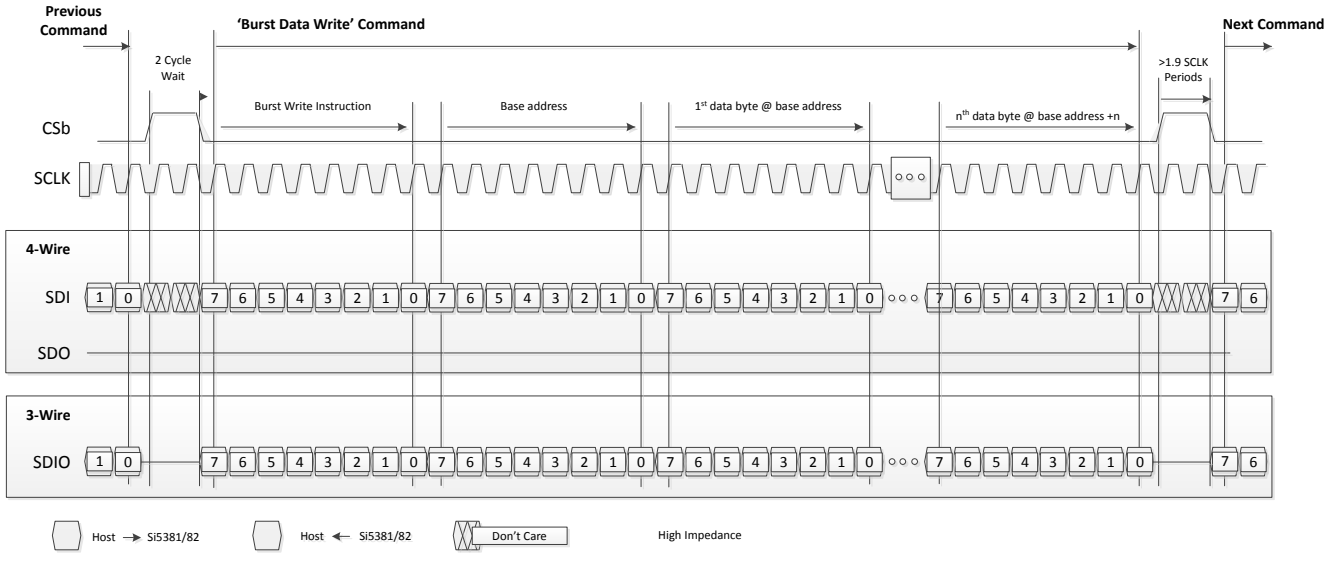


Figure 7.12. SPI "Burst Data Write" Instruction Timing

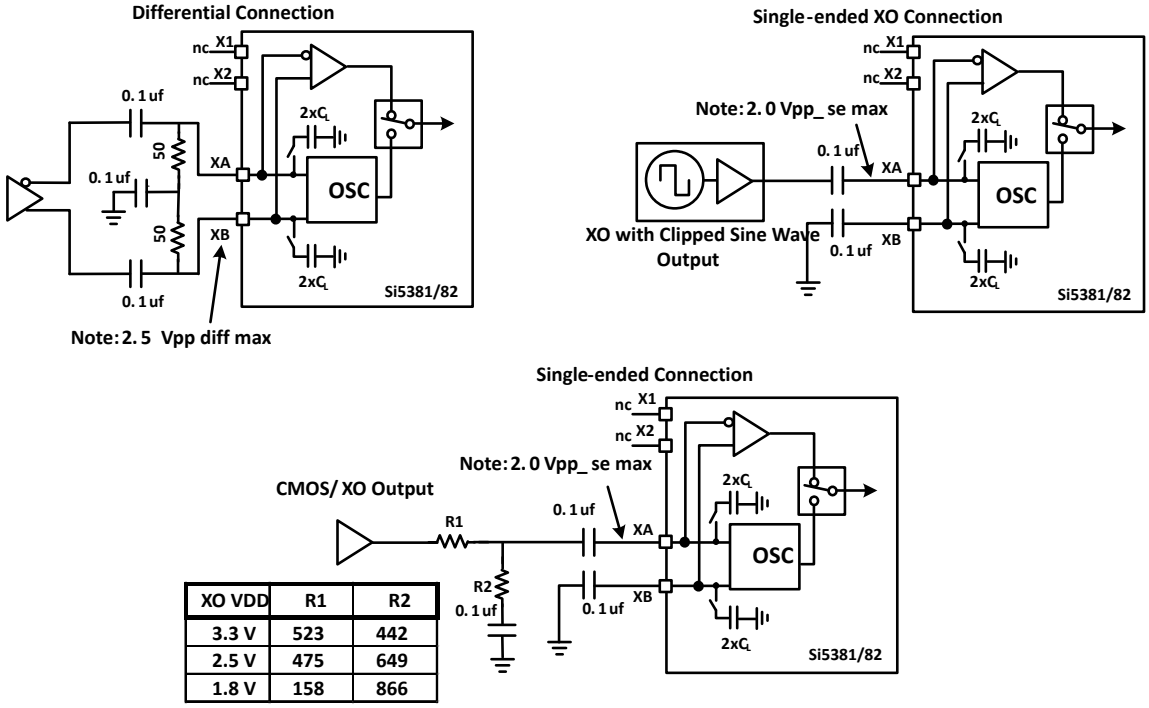
8. Field Programming

To simplify design and software development of systems using the Si5381/82, a field programmer is available. The ClockBuilder Pro Field Programmer supports both “in-system” programming for devices already mounted on a PCB, as well as “in-socket” programming of Si5381/82 sample devices. Refer to http://www.silabs.com/CBProgrammer for information about this kit.

9. XAXB External References

9.1 Performance of External References

An external crystal oscillator (XO) is required to set the reference for the Si5381/82. Either a 54 MHz or 48.0231 MHz XO may be used as the reference to the wireless jitter attenuator.



XO VDD	R1	R2
3.3 V	523	442
2.5 V	475	649
1.8 V	158	866

Figure 9.1. XAXB External Reference Clock Connection Options

The Si5381/82 accepts a Clipped Sine wave, CMOS, or Differential reference clock on the XAXB interface. Most clipped sine wave and CMOS TCXOs have insufficient drive strength to drive a 50 Ω or 100 Ω load. For this reason, place the TCXO as close to the Si5381/82 as possible to minimize PCB trace length. In addition, connect both the Si5381/82 and the TCXO directly to the same ground plane. The figure above shows the recommended method of connecting a clipped sine wave TCXO to the Si5381/82. Because the Si5381/82 provides dc bias at the XA and XB pins, the ~800 mV peak-peak swing can be input directly into XA after ac-coupling. Single-ended inputs must be connected to the XA pin with proper termination on the XB pin. Because the signal is single-ended in this case, the XB input is ac-coupled to ground. The figure above also illustrates the recommended method of connecting a single-ended CMOS rail-to-rail output to the XAXB inputs of the Si5381/82. The resistor network attenuates the swing to ensure that the maximum input voltage swing at the XA pin remains below the datasheet specification. The signal is ac-coupled before connecting it to the Si5381/82 XA input with the XB input again AC grounded through a capacitor. For applications with loop bandwidth values less than 10 Hz that require low wander output clocks, using an external TCXO as the XAXB reference source should be considered to avoid the wander of a crystal or regular XO.

9.2 Recommended Reference Oscillators

The Si5381/82 can use either 54 MHz or 48.0231 MHz reference XOs. This should be a high-quality “low phase noise” or “ultra-low phase noise” type to reduce phase noise on the output clocks. See the table below for a list of some recommended XOs to use with this device. Other XOs with similar performance at these frequencies may be used also. Please contact Silicon Labs Technical Support with questions on XAXB reference frequencies, tolerances, or other XO performance specifications.

Table 9.1. Recommended LTE Reference XOs

Supplier	Part Number	Frequency (MHz)	Typ 100 Hz	Stability over PN (dBc/Hz)	Aging Temp (ppm)	Temp (ppm/yr.) (degC)	Package (mm x mm)	Supply (V)	Typ Current (mA)
TXC	7X54000007	54	-118	±50	±3	-40 to +105	3.2 x 2.5	3.3	13
AccuSilicon	AS318-B-480231	48.0231	-129	±50	±3	-40 to +105	2.5 x 2.0	3.3	11

10. XO and Device Circuit Layout Recommendations

The main layout issues that should be carefully considered for optimum phase noise include the following:

- Number and size of the ground/thermal vias for the Epad (see 11.4 Grounding Vias)
- Output clock trace routing
- Input clock trace routing
- Control and Status signals to input or output clock trace coupling

Si5381A-E-EVB and Si5382A-E-EVB schematics, layouts, and component BOM files are available at: http://www.silabs.com/Si538x-4x-EVB

10.1 Si5381/82 64-Pin QFN with External XO Layout Recommendations

This section details the recommended guidelines for the layout of the 64-pin QFN Si5381/82 with external XO using the 8-layer Si5381A-E-EB PCB. The following are the descriptions of each of the eight layers.

- Layer 1: device layer, with low speed CMOS control/status signals, ground flooded
- Layer 2: input clocks, ground flooded
- Layer 3: ground plane
- Layer 4: power distribution, ground flooded
- Layer 5: power routing layer
- Layer 6: ground input clocks, ground flooded
- Layer 7: output clocks layer
- Layer 8: ground layer

External XO: The figure below shows the top layer layout of the Si5381/82 device mounted on the PCB. The XO is outlined with the white box around it. The top layer is flooded with ground. Both the XA and XB pins are capacitively coupled, with XB ac connected to XO ground for single-ended output XO's. Notice the 5x5 array of thermal vias in the center of the device. See for more information on thermal/ground via layout.

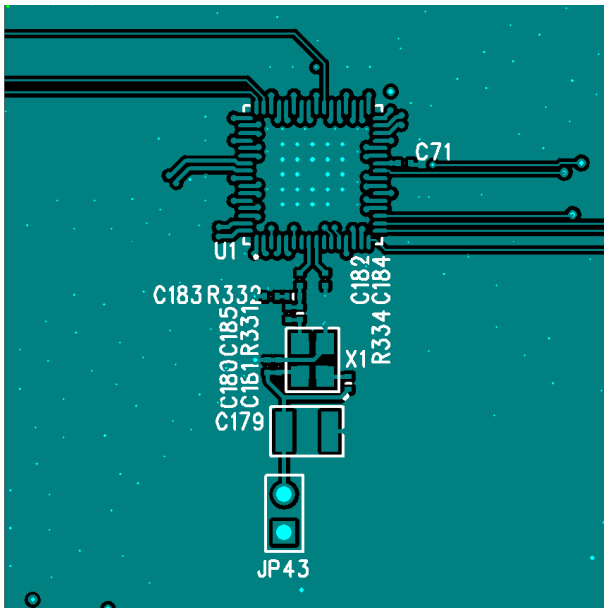


Figure 10.1. External XO: Si5381/82 Device and XO Layout Recommendations, Top Layer (Layer 1)

External XO: The following figure shows the layer that implements the ground shield underneath the XO. This layer also has the clock input pins. The clock input pins go to layer 2 using vias to avoid crosstalk. As soon as the clock inputs are on layer 2, they have a ground shield above, below, and on the sides for maximum protection.

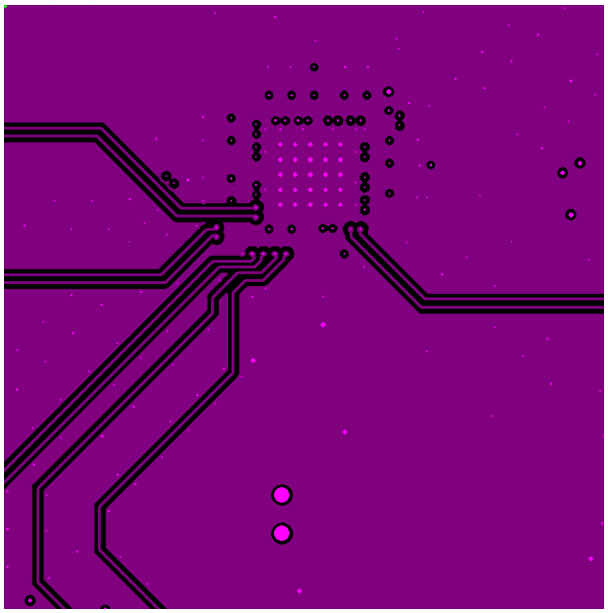


Figure 10.2. External XO: Input Clocks and Ground Fill, Below the Top Layer (Layer 2)

External XO: The figure below shows one of the ground planes. Figure 10.4 External XO: Internal Power Plane (Layer 4) on page 75 is a power plane and shows the clock output power supply traces.

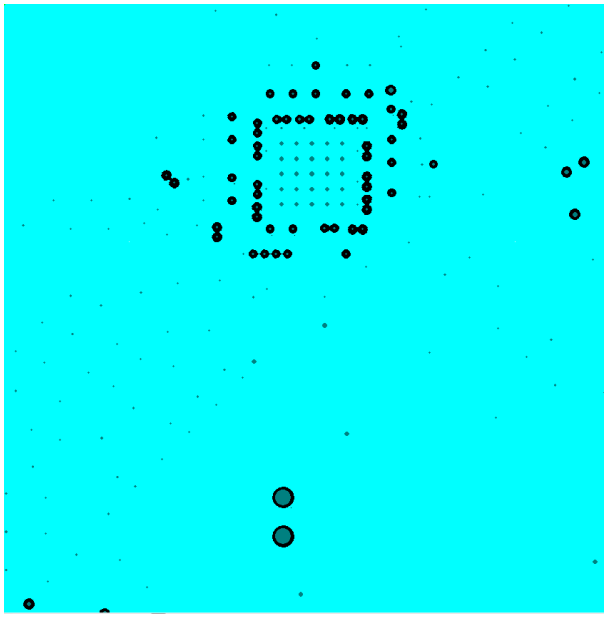


Figure 10.3. External XO: Internal Ground Plane (Layer 3)

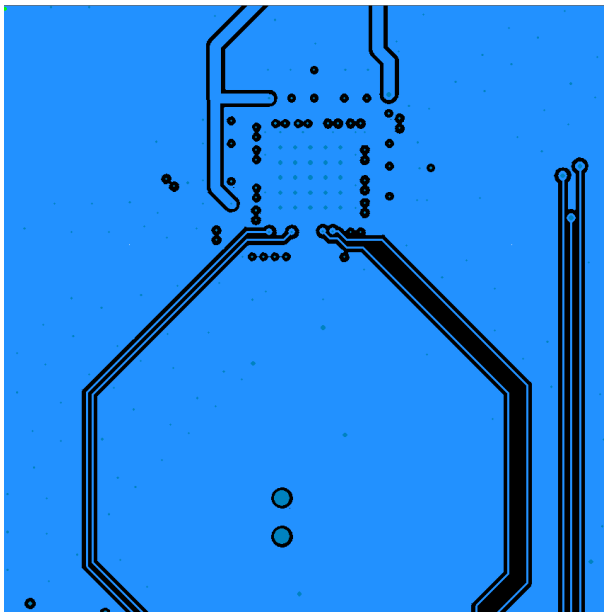


Figure 10.4. External XO: Internal Power Plane (Layer 4)

External XO: The figure below shows layer 5, which is the power plane routed to the clock output power pins.

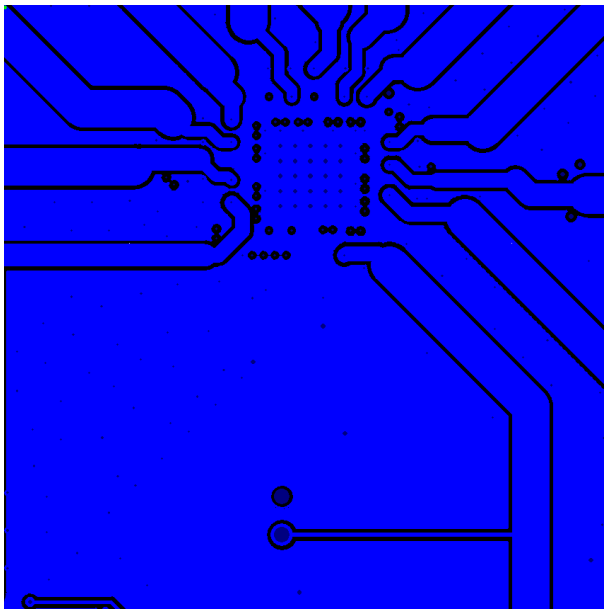


Figure 10.5. External XO: Internal Power Plane (Layer 5)

External XO: The figure below shows layer 6, another ground plane similar to layer 3.

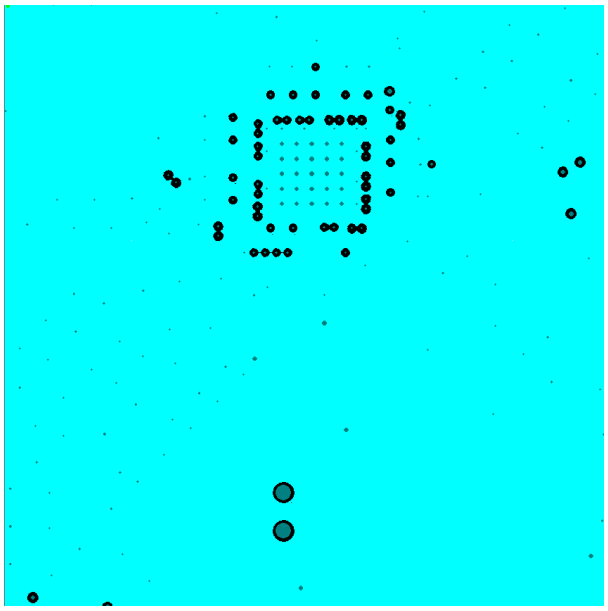


Figure 10.6. External XO: Internal Ground Plane (Layer 6)

External XO: The figure below shows the output clocks. Similar to the input clocks, the output clocks have vias that immediately go to a buried layer with a ground plane above them and a ground flooded bottom layer. There is ground flooding between the clock output pairs to reduce crosstalk. There should be a line of vias through the ground flood on either side of the output clocks to ensure that the ground flood immediately next to the differential pairs has a low inductance path to the ground plane on layers 3 and 6.

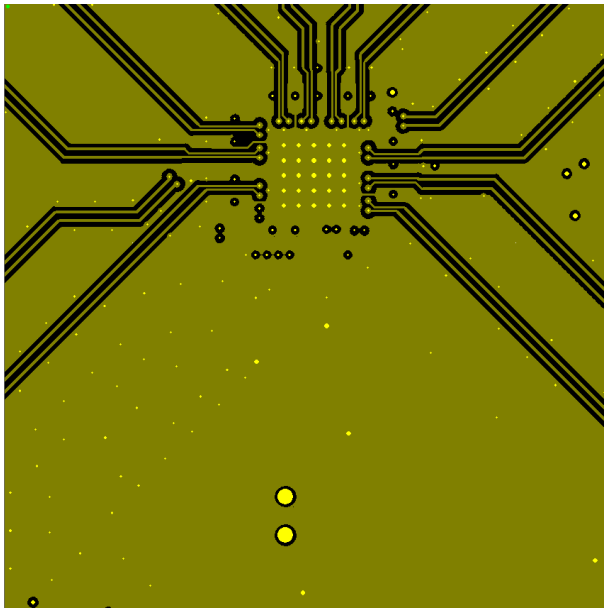


Figure 10.7. External XO: Output Clocks (Layer 7)

External XO: The bottom layer shown in the figure below displays the location of the decoupling capacitors close to the device.

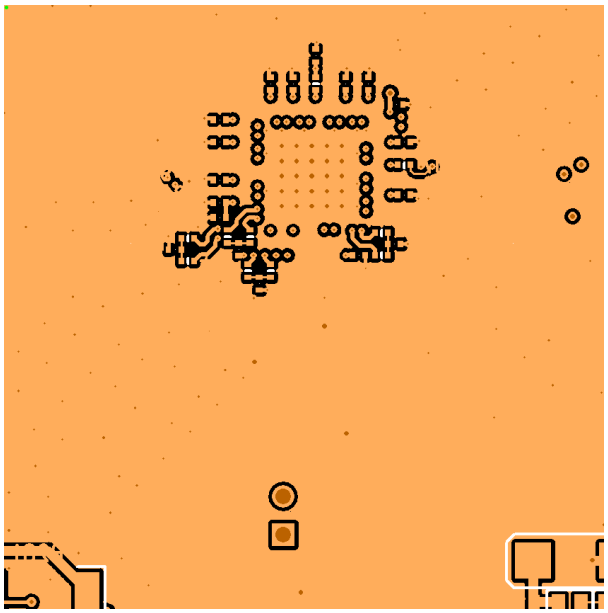


Figure 10.8. External XO: Bottom Layer Ground Flooded (Layer 8)

11. Power Management

11.1 Power Management Features

A number of unused functions can be powered down to minimize power consumption. The registers listed in the table below are used for powering down different features of the device.

Table 11.1. Powerdown Registers

Register Name	Hex Address [Bit Field]	Function
PDN	0x001E[0]	Place the device into a low current Powerdown state. Note that the serial interface and registers remain active in this state. 0: Normal Operation (default) 1: Powerdown Device
OUT0A_PDN OUT0_PDN OUT1_PDN OUT2_PDN OUT3_PDN OUT4_PDN OUT5_PDN OUT6_PDN OUT7_PDN OUT8_PDN OUT9_PDN OUT9A_PDN	0x0103[0] 0x0108[0] 0x010D[0] 0x0112[0] 0x0117[0] 0x011C[0] 0x0121[0] 0x0126[0] 0x012B[0] 0x0130[0] 0x0135[0] 0x013A[0]	Powers down unused output drivers. 0: Power-up output driver (default) 1: Powerdown output driver When powered down, output pins will be high impedance with a light pull down effect.
OUT_PDN_ALL	0x0145[0]	Powers down all output drivers. 0: Normal Operation (default) 1: Powerdown All output drivers
IN_EN	0x0949[3:0]	Enable (or powerdown) the IN3/FB_IN - IN0 input buffers. 0: Powerdown input buffer 1: Enable and Power-up input buffer

11.2 Power Supply Recommendations

Power supply filtering is generally important for optimal timing performance. The Si5381/82 devices have multiple stages of on-chip regulation to minimize the impact of board level noise on clock jitter. Following conventional power supply filtering and layout techniques will minimize signal degradation from power supply noise.

It is recommended to use a 0402-size 1 mF ceramic capacitor on each power supply pin for optimal performance. If the supply voltage is extremely noisy, it might require a ferrite bead in series between the voltage supply voltage and the device power supply pin.

11.3 Power Supply Sequencing

Four classes of supply voltages exist on the Si5381/82:

1. VDD=1.8V (Core digital supply)
2. VDDA=3.3V (Analog supply)
3. VDDO=1.8/2.5/3.3V (Output Clock supplies)

There is no general requirement for power supply sequencing on this device unless the output clocks are required to be phase aligned with each other. In this case, the VDDO of each clock which needs to be aligned must be powered up before VDD and VDDA.

If output-to-output alignment is required for applications where it is not possible to properly sequence the power supplies, then the output clocks can be aligned by asserting Hard Reset 0x001E[1] register bits or driving the RSTb pin. Note that using a Hard Reset will reload the register with the contents of the NVM and any unsaved register changes will be lost.

One may observe that when powering up the VDD = 1.8V rail first, that the VDDA = 3.3V rail will initially follow the 1.8V rail. Likewise, if the VDDA rail is powered down first then it will not drop far below VDD until VDD itself is powered down. This is due to the pad I/O circuits which have large MOSFET switches to select the local supply from either the VDD or VDDA rails. These devices are relatively large and yield a parasitic diode between VDD and VDDA. Please allow for both VDD and VDDA to power-up and power-down before measuring their respective voltages.

11.4 Grounding Vias

The "Epad" on the bottom of the device functions as both the sole electrical ground and as the primary heat transfer path. Hence it is important to minimize the inductance and maximize the heat transfer from this pad to the internal ground plane of the PCB. Use no fewer than 25 vias from the center pad to a ground plane under the device. In general, more vias will perform better. Having the ground plane near the top layer will also help to minimize the via inductance from the device to ground and maximize the heat transfer away from the device.

12. Base vs. Factory Preprogrammed Devices

The Si5381/82 devices can be ordered as "base" or "factory-preprogrammed" (also known as "custom OPN") versions.

12.1 "Base" Devices (a.k.a. "Blank" Devices)

- Example "base" orderable part numbers (OPNs) are of the form "Si5381A-E-GM."
- Base devices are available for applications where volatile reads and writes are used to program and configure the device for a particular application.
- Base devices do not power up in a usable state (all output clocks are disabled).
- Base devices are, however, configured by default to use a 1.8 V compatible I/O voltage setting for the host I^2C/SPI interface and external 54 MHz XO as the reference clock by default.
- Additional programming of a base device is mandatory to achieve a usable configuration.
- See the on-line lookup utility at www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx to access the default configuration plan and register settings for any base OPN.

12.2 "Factory Preprogrammed" (Custom OPN) Devices

- Factory preprogammed devices use a “custom OPN”, such as Si5382A-Exxxxx-GM, where “xxxxx” is a sequence of characters assigned by Silicon Labs for each customer-specific configuration. These characters are referred to as the “OPN ID”. Customers must initiate custom OPN creation using the ClockBuilder Pro software.
- Many customers prefer to order devices which are factory preprogrammed for a particular application that includes specifying the clock input frequencies, the clock output frequencies, as well as the other options, such as automatic clock selection, loop BW, etc. The ClockBuilder software is required to select among all of these options and to produce a project file which Silicon Labs uses to preprogram all devices with custom orderable part number (“custom OPN”).
- Custom OPN devices contain all of the initialization information in their non-volatile memory (NVM) so that it powers up fully configured and ready to go.
- Because preprogrammed device applications are inherently quite different from one another, the default power up values of the register settings can be determined using the custom OPN utility at: http://www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx
- Custom OPN devices include a device top mark which includes the unique OPN ID. Refer to the device data sheet's Ordering Guide and Top Mark sections for more details.

Both "base" and "factory preprogrammed" devices can have their operating configurations changed at any time using volatile reads and writes to the registers. Both types of devices can also have their current register configuration written to the NVM by executing an NVM bank burn sequence (see 2.1.2 NVM Programming).

12.3 Part Numbering Summary

Part numbers are of the form:

Si<Part Num Type><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

For example:

- **Si5381A-E12346-GM:** Applies to a factory preprogrammed OPN (Ordering Part Number) device. These devices are programmed at the factory with the frequency plan and all other operating characteristics defined by the user's ClockBuilder Pro project file.
- **Si5382A-E-GM:** Applies to a "base" device. Base devices are factory programmed to a specific base part type (e.g., Si5381/82) but **exclude** any user-defined frequency plan or other operating characteristics which would be selected in ClockBuilder Pro.

13. Si5381 Register Map

13.1 Page 0 Registers

Table 13.1. Register 0x0000 Die Rev

Reg Address	Bit Field	Type	Name	Default	Description
0x0000	3:0	R	DIE_REV	0	4-bit die revision number.

Table 13.2. Register 0x0001 Page

Reg Address	Bit Field	Type	Name	Default	Description
0x0001	7:0	R/W	PAGE	0	Select one of 256 possible pages.

This is the “Page Register” which is located at address 0x01 on every page. When read, it will indicate the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, ... See application note, "AN926: Reading and Writing Registers with SPI and I2C for Si534x/8x Devices".

Table 13.3. Register 0x0002-0x0003 Base Part Number

Reg Address	Bit Field	Type	Name	Default	Description
0x0002	7:0	R	PN_BASE	0x81	Four-digit ,"base" part number, one nibble per digit. Example: Si5381A-E12346-GM. The base part number (OPN) is 5381, which is stored in this register.
0x0003	15:8	R	PN_BASE	0x53	

See 12.3 Part Numbering Summary for more information on part numbers.

Table 13.4. Register 0x0004 Device Grade

Reg Address	Bit Field	Type	Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed grade. 0 = A, 1 = B, 2 = C, 3 = D, 4 = E, etc. For example in Si5381A-E12346-GM, the GRADE is A = 0

See 12.3 Part Numbering Summary for more information on part numbers. Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 13.5. Register 0x0005 Device Revision

Reg Address	Bit Field	Type	Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B; 2 = C, 3 = D, 4 = E, etc. For example in Si5381A-E12346-GM, the device revision is E = 4

See 12.3 Part Numbering Summary for more information on part numbers. Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 13.6. Register 0x0009 Temperature Grade

Reg Address	Bit Field	Type	Name	Description
0x0009	7:0	R	TEMP_GRADE	Device temperature grade: 0: Industrial (-40 to 85 °C

See 12.3 Part Numbering Summary for more information on part numbers.

Table 13.7. Register 0x000A Package ID

Reg Address	Bit Field	Type	Name	Description
0x000A	7:0	R	PKG_ID	Package Identifier: 0: 64-pin 9x9 mm QFN

See 12.3 Part Numbering Summary for more information on part numbers.

Table 13.8. Register 0x000B I2C Address

Reg Address	Bit Field	Type	Name	Description
0x000B	6:0	R	I2C_ADDR	7-bit I2C Address

Note that the two least significant bits, [1:0], are determined by the voltages on the A1 and A0 input pins respectively. This setting is not saved as part of the usual NVM write procedure. To update this register in a non-volatile way, the "Si534x8x I2C Address Burn Tool" allows updating this value one time. This utility is included in the ClockBuilder Pro installation and can be accessed under the "Misc" folder in the installation directory.

Table 13.9. Register 0x000C Device Status

Reg Address	Bit Field	Type	Name	Description
0x000C	0	R	SYSINCAL	1 if the device is currently calibrating.
0x000C	1	R	LOSXAXB	1 if there is currently no signal from the XAXB reference clock.
0x000C	2	R	LOSREF	1 if there is currently no signal detected from the XAXB reference clock.
0x000C	3	R	XAXB_ERR	1 if there is currently a problem locking to the XAXB reference clock.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is currently an SMB Bus Timeout error.

See 3.3 Fault Monitoring for more information.

Table 13.10. Register 0x000D Out-of-Frequency (OOF) and Loss-of Signal (LOS) Status

Reg Address	Bit Field	Type	Name	Description
0x000D	3:0	R	LOS	1 if [IN3 - IN0] is currently LOS

Reg Address	Bit Field	Type	Name	Description
0x000D	7:4	R	OOF	1 if [IN3 - IN0] is currently OOF

See 3.3 Fault Monitoring for more information.

- IN0: LOS 0x000D[0], OOF 0x000D[4]
- IN1: LOS 0x000D[1], OOF 0x000D[5]
- IN2: LOS 0x000D[2], OOF 0x000D[6]
- IN3: LOS 0x000D[3], OOF 0x000D[7]

Table 13.11. Register 0x000E Holdover (HOLD) and Loss-of-Lock (LOL) Status

Reg Address	Bit Field	Type	Name	Description
0x000E	3:0	R	LOL_PLL[D:A]	1 if the DSPLL[D:A] is currently out of lock
0x000E	7:4	R	HOLD_PLL[D:A]	1 if the DSPLL[D:A] is currently in Holdover or Freerun

See 3.3 Fault Monitoring for more information.

Table 13.12. Register 0x000F DSPLL Calibration Status

Reg Address	Bit Field	Type	Name	Description
0x000F	7:4	R	CAL_PLL[D:A]	1 if the DSPLL[D:A] internal calibration is currently busy

See 3.3 Fault Monitoring for more information.

Table 13.13. Register 0x0011 Device Status Flags

Reg Address	Bit Field	Type	Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Flag 1 if the device was or is in SYSINCAL
0x0011	1	R/W	LOSXAXB_FLG	Flag 1 if the XAXB reference clock was or is LOSXAXB
0x0011	2	R/W	LOSREF_FLG	Flag 1 if XAXB reference clock was or isLOSREF
0x0011	3	R/W	XAXB_ERR_FLG	Flag 1 if XAXB reference clock was or is XAXB_ERR
0x0011	5	R/W	SMB_TMOUT_FLG	Flag 1 if SMB_TMOUT was or is in error

These are sticky flag bits corresponding to the bits in register 0x000C. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000C register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

Table 13.14. Register 0x0012 OOF and LOS Status Flags

Reg Address	Bit Field	Type	Name	Description
0x0012	3:0	R/W	LOS_FLG	Flag 1 if [IN3 - IN0] was or is LOS
0x0012	7:4	R/W	OOF_FLG	Flag 1 if [IN3 - IN0] was or is OOF

These are sticky flag bits corresponding to the bits in register 0x000D. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000D register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

- IN0: LOS_FLG 0x0012[0], OOF_FLG 0x0012[4]
- IN1: LOS_FLG 0x0012[1], OOF_FLG 0x0012[5]
- IN2: LOS_FLG 0x0012[2], OOF_FLG 0x0012[6]
- IN3: LOS_FLG 0x0012[3], OOF_FLG 0x0012[7]

Table 13.15. Register 0x0013 HOLD and LOL Status Flags

Reg Address	Bit Field	Type	Name	Description
0x0013	3:0	R/W	LOL_FLG_PLL[D:A]	Flag 1 if the DSPLL was or is LOL
0x0013	7:4	R/W	HOLD_FLG_PLL[D:A]	Flag 1 if the DSPLL was or is in Holdover or Freerun

These are sticky flag bits corresponding to the bits in register 0x000E. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000E register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

Table 13.16. Register 0x0014 DSPLL Calibration Status Flag

Reg Address	Bit Field	Type	Name	Description
0x0014	7:4	R/W	CAL_FLG_PLL[D:A]	Flag 1 if the internal calibration was or is busy

These are sticky flag bits corresponding to the bits in register 0x000F. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000F register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

Table 13.17. Register 0x0017 Device Status Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_FLG_MSK	1 to mask LOSXAXB_FLG from causing an interrupt
0x0017	2	R/W	LOSREF_INTR_MSK	1 to mask LOSREF_FLG from causing an interrupt
0x0017	3	R/W	XAXB_ERR_INTR_MSK	1 to mask LOL_FLG from causing an interrupt
0x0017	5	R/W	SMBUS_IMOUT_ FLG_MSK	1 to mask SMBUS_TMOUT_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0011. See 3.3.6 INTRb Interrupt Configuration for more information.

Table 13.18. Register 0x0018 OOF and LOS Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1 to mask LOS_FLG from causing an interrupt
0x0018	7:4	R/W	OOF_INTR_MSK	1 to mask OOF_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0012. See 3.3.6 INTRb Interrupt Configuration for more information.

- IN0: LOS_INTR_MSK 0x0018[0], OOF_INTR_MSK 0x0018[4]

- IN1: LOS_INTR_MSK 0x0018[1], OOF_INTR_MSK 0x0018[5]
- IN2: LOS_INTR_MSK 0x0018[2], OOF_INTR_MSK 0x0018[6]
- IN3: LOS_INTR_MSK 0x0018[3], OOF_INTR_MSK 0x0018[7]

Table 13.19. Register 0x0019 HOLD and LOL Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0019	3:0	R/W	LOL_INTR_MSK_PLL[D:A]	1 to mask LOL_FLG from causing an interrupt
0x0019	7:4	R/W	HOLD_INTR_MSK_PLL[D:A]	1 to mask HOLD_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0013. See 3.3.6 INTRb Interrupt Configuration for more information.

Table 13.20. Register 0x001A PLL In Calibration Interrupt Mask

Reg Address	Bit Field	Type	Name	Description
0x001A	7:4	R/W	CAL_INTR_MSK_PLL[D:A]	1 to mask CAL_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0014. See 3.3.6 INTRb Interrupt Configuration for more information.

Table 13.21. Register 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Name	Description
0x001C	0	S	SOFT_RST	1: Initializes and calibrates the entire device 0: No effect
0x001C	1	S	SOFT_RST_PLLA	1: Initializes and calibrates DSPLLA 0: No effect
0x001C	2	S	SOFT_RST_PLLB	1: Initializes and calibrates DSPLLB 0: No effect
0x001C	3	S	SOFT_RST_PLLC	1: Initializes and calibrates DSPLLC 0: No effect
0x001C	4	S	SOFT_RST_PLLD	1: Initializes and calibrates DSPLLD 0: No effect

Soft Reset restarts the device using the existing register values without loading from NVM. Soft Reset also updates registers requiring a separate update strobe, including the DSPLL bandwidth registers as well as the P, M, N, and R dividers. Unlike SOFT_RST_ALL, the SOFT_RST_PLLx bits do not update the loop BW values. If these have changed, the update can be done by writing to BW_UPDATE_PLLA, BW_UPDATE_PLLB, BW_UPDATE_PLLC, and BW_UPDATE_PLLD at addresses 0x0414, 0x0514, 0x0614, and 0x0715.

Table 13.22. Register 0x001D FINC, FDEC DCO Controls for DSPLLs A/C/D

Reg Address	Bit Field	Type	Name	Description
0x001D	0	S	FINC	0: No effect 1: A rising edge will cause an frequency increment for DSPLL A/C/D when the N_FSTEP_MSK bits are 0.
0x001D	1	S	FDEC	0: No effect 1: A rising edge will cause an frequency decrement for DSPLL A/C/D when the N_FSTEP_MSK bits are 0.

Table 13.23. Register 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Name	Description
0x001E	0	R/W	PDN	Place the device into a low current Powerdown state. Note that the serial interface and registers remain active in this state. The DSPLLs will need to re-acquire lock when exiting this state. 0: Normal Operation (default) 1: Powerdown Device
0x001E	1	S	HARD_RST	Perform Hard Reset with NVM read. 0: Normal Operation 1: Hard Reset the device
0x001E	2	S	SYNC	Resets all R dividers. Logically equivalent to asserting the SYNCb pin. 0: Normal Operation 1: Reset R Dividers

Table 13.24. Register 0x0020 DSPLL_SEL[1:0] Control of FINC/FDEC for DCO

Reg Address	Bit Field	Type	Name	Description
0x0020	0	R/W	FSTEP_PLL_SINGLE	0: FSTEP_PLL bits are disabled. 1: DSPLL_SEL[1:0] FSTEP_PLL bits are enabled. See FSTEP_PLL_REGCTRL below.
0x0020	1	R/W	FSTEP_PLL_REGCTRL	Only active when FSTEP_PLL_SINGLE = 1. 0: FSTEP_PLL bits are disabled. 1: FSTEP_PLL bits are enabled.

Reg Address	Bit Field	Type	Name	Description
0x0020	3:2	R/W	FSTEP_PLL[1:0]	Used to select which PLL (M divider) is affected by FINC/FDEC. 0: DSPLL A M-divider 1: Reserved 2: DSPLL C M-divider 3: DSPLL D M-divider

Table 13.25. Register 0x0022 Output Enable Group Controls

Reg Address	Bit Field	Type	Name	Description
0x0022	0	R/W	OE_REG_SEL	Selects between Pin and Register control for output disable. 0: OEb Pin disable (default) 1: OE Register disable
0x0022	1	R/W	OE_REG_DIS	When OE_REG_SEL = 1: 0: Disable selected outputs 1: Enable selected outputs

By default ClockBuilder Pro sets the OEb pin controlling all outputs. OUTALL_DISABLE_LOW (0x0102[0]) must be high (enabled) to allow the OEb pin to enable outputs. Note that the OE_REG_DIS bit (active high) has inverted logic sense from the OEb pin (active low). See 4.7.5 Output Driver Disable Source Summary for more information.

Table 13.26. Register 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Name	Description
0x002B	3	R/W	SPI_3WIRE	Selects operating mode for SPI interface: 0: 4-wire SPI (default) 1: 3-wire SPI

This bit is ignored for I2C bus operation, when I2C_SEL is high. The SPI_3WIRE setting may be updated by either 3-wire or 4-wire writes, since the same 3 pins are used in either mode. When changing this setting the serial interface will be ready to read registers on the next command. 4-wire mode (0x002B=0x0) is the safe default choice to avoid possible contention on the bi-directional 3-wire data pin.

Table 13.27. Register 0x002C LOS Enables

Reg Address	Bit Field	Type	Name	Description
0x002C	3:0	R/W	LOS_EN	Enable LOS detection on IN3 - IN0. 0: Disable LOS Detection 1: Enable LOS Detection
0x002C	4	R/W	LOSXAXB_DIS	Enable LOS detection on the XAXB reference clock. 0: Enable LOS Detection (default). 1: Disable LOS Detection.

- IN0: LOS_EN[0]
- IN1: LOS_EN[1]
- IN2: LOS_EN[2]
- IN3: LOS_EN[3]

Table 13.28. Register 0x002D LOS Clear Delays

Reg Address	Bit Field	Type	Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	IN0 LOS Clear delay. 0: 2 ms 1: 100 ms 2: 200 ms 3: 1000 ms
0x002D	3:2	R/W	LOS1_VAL_TIME	IN1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	IN2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	IN3, same as above

When a valid input clock is not present on the input, LOS will be asserted. When the clock returns, it must remain valid for this period of time before that clock is considered to be qualified again.

Table 13.29. Register 0x002E-0x002F IN0 LOS Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit LOS Trigger Threshold value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value, given a particular frequency plan.

Table 13.30. Register 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit LOS Clear Threshold value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold, given a particular frequency plan.

All four input buffers are identical in terms of control. The single set of descriptions for IN0 above also apply to IN1-IN3.

Table 13.31. Output Registers Following the Same Definitions as IN0

Register Addresses	Description	(Same as) Addresses
0x0030 - 0x0031	IN1 LOS Trigger Threshold	0x002E - 0x002F
0x0038 - 0x0039	IN1 LOS Clear Threshold	0x002E - 0x002F
0x0032 - 0x0033	IN2 LOS Trigger Threshold	0x002E - 0x002F
0x003A - 0x003B	IN2 LOS Clear Threshold	0x002E - 0x002F
0x0034 - 0x0035	IN3 LOS Trigger Threshold	0x002E - 0x002F
0x003C - 0x003D	IN3 LOS Clear Threshold	0x002E - 0x002F

Table 13.32. Register 0x003E LOS Min Period Enable

Reg Address	Bit Field	Type	Name	Description
0x003E	7:4	R/W	LOS_MIN_PERI-OD_EN	Values set by CBPro.

Table 13.33. Register 0x003F OOF Enable

Reg Address	Bit Field	Type	Name	Description
0x003F	3:0	R/W	OOF_EN	Enable Precision OOF for IN3 - IN0 0: Disable Precision OOF 1: Enable Precision OOF
0x003F	7:4	R/W	FAST_OOF_EN	Enable Fast OOF for IN3 - IN0 0: Disable Fast OOF 1: Enable Fast OOF

- IN0: OOF_EN[0], FAST_OOF_EN[4]
- IN1: OOF_EN[1], FAST_OOF_EN[5]
- IN2: OOF_EN[2], FAST_OOF_EN[6]
- IN3: OOF_EN[3], FAST_OOF_EN[7]

Table 13.34. Register 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	Select reference 0ppm 0: IN0 1: IN1 2: IN2 3: IN3 4: XAXB reference clock (default) 5-7: Reserved

Table 13.35. Register 0x0041 OOF0 Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0041	4:0	R/W	OOF0_DIV_SEL	Values calculated by CBPro.

Table 13.36. Register 0x0042 OOF1 Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0042	4:0	R/W	OOF1_DIV_SEL	Values calculated by CBPro.

Table 13.37. Register 0x0043 OOF2 Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0043	4:0	R/W	OOF2_DIV_SEL	Values calculated by CBPro.

Table 13.38. Register 0x0044 OOF3 Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0044	4:0	R/W	OOF3_DIV_SEL	Values calculated by CBPro.

Table 13.39. Register 0x0045 OOFXO Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0045	4:0	R/W	OOFXO_DIV_SEL V	Values calculated by CBPro.

Table 13.40. Register 0x0046-0x0049 Precision OOF Set Thresholds

Reg Address	Bit Field	Type	Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	Precision OOF Set Threshold. The range is from ±2 ppm to ±510 ppm in 2 ppm steps. Set Threshold (ppm) = OOFx_SET_THR x 2 ppm OOF will be continuously indicated if this is set to 0.
0x0047	7:0	R/W	OOF1_SET_THR	
0x0048	7:0	R/W	OOF2_SET_THR	
0x0049	7:0	R/W	OOF3_SET_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 13.41. Register 0x004A-0x004D Precision OOF Clear Thresholds

Reg Address	Bit Field	Type	Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	Precision OOF Clear Threshold. The range is from ±2 ppm to ±510 ppm in 2 ppm steps. Clear Threshold (ppm) = OOFx_CLR_THR x ±2 ppm Note that OOF will be continuously indicated if this is set to 0.
0x004B	7:0	R/W	OOF1_CLR_THR	
0x004C	7:0	R/W	OOF2_CLR_THR	
0x004D	7:0	R/W	OOF3_CLR_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 13.42. Register 0x004E–0x004F OOF Detection Windows

Reg Address	Bit Field	Type	Name	Description
0x004E	2:0	R/W	FAST_OOF0_DETWIN_SEL	Values calculated by CBPro.
0x004E	6:4	R/W	FAST_OOF1_DETWIN_SEL	
0x004F	2:0	R/W	FAST_OOF2_DETWIN_SEL	
0x004F	6:4	R/W	FAST_OOF3_DETWIN_SEL	

Table 13.43. Register 0x0050 OOF on LOS Controls

Reg Address	Bit Field	Type	Name	Description
0x0050	3:0	R/W	OOF_ON_LOS	Values set by CBPro.

Table 13.44. Register 0x0051-0x0054 Fast OOF Set Thresholds

Reg Address	Bit Field	Type	Name	Description
0x0051	3:0	R/W	FAST_OOF0_SET_THR	Fast OOF Set Threshold. The range is from ±1,000 ppm to ±16,000 ppm in 1000 ppm steps. Fast Set Threshold (ppm) = (FAST_OOFx_SET_THR + 1) x ±1000 ppm Note that OOF will be continuously indicated if this is set to 0.
0x0052	3:0	R/W	FAST_OOF1_SET_THR	
0x0053	3:0	R/W	FAST_OOF2_SET_THR	
0x0054	3:0	R/W	FAST_OOF3_SET_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 13.45. Register 0x0055-0x0058 Fast OOF Clear Thresholds

Reg Address	Bit Field	Type	Name	Description
0x0055	3:0	R/W	FAST_OOF0_CLR_THR	Fast OOF Clear Threshold. The range is from ±1,000 ppm to ±16,000 ppm in 1000 ppm steps. Fast Clear Threshold (ppm) = (FAST_OOFx_CLR_THR + 1) * ±1000ppm Note that OOF will be continuously indicated if this is set to 0.
0x0056	3:0	R/W	FAST_OOF1_CLR_THR	
0x0057	3:0	R/W	FAST_OOF2_CLR_THR	
0x0058	3:0	R/W	FAST_OOF3_CLR_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 13.46. Register 0x0059 Fast OOF Detection Window

Reg Address	Bit Field	Type	Name	Description
0x0059	1:0	R/W	FAST_OOF0_DETWIN_SEL	Values calculated by CBPro.
0x0059	3:2	R/W	FAST_OOF1_DETWIN_SEL	
0x0059	5:4	R/W	FAST_OOF2_DETWIN_SEL	
0x0059	7:6	R/W	FAST_OOF3_DETWIN_SEL	

Table 13.47. Register 0x005A–0x005D OOF0 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x005A	7:0	R/W	OOF0_RATIO_REF	Values calculated by CBPro.
0x005B	15:8	R/W	OOF0_RATIO_REF	
0x005C	23:16	R/W	OOF0_RATIO_REF	
0x005D	25:24	R/W	OOF0_RATIO_REF	

Table 13.48. Register 0x005E–0x0061 OOF1 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x005E	7:0	R/W	OOF1_RATIO_REF	Values calculated by CBPro.
0x005F	15:8	R/W	OOF1_RATIO_REF	
0x0060	23:16	R/W	OOF1_RATIO_REF	
0x0061	25:24	R/W	OOF1_RATIO_REF	

Table 13.49. Register 0x0062–0x0065 OOF2 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x0062	7:0	R/W	OOF2_RATIO_REF	Values calculated by CBPro.
0x0063	15:8	R/W	OOF2_RATIO_REF	
0x0064	23:16	R/W	OOF2_RATIO_REF	
0x0065	25:24	R/W	OOF2_RATIO_REF	

Table 13.50. Register 0x0066–0x0069 OOF3 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x0066	7:0	R/W	OOF3_RATIO_REF	Values calculated by CBPro.
0x0067	15:8	R/W	OOF3_RATIO_REF	
0x0068	23:16	R/W	OOF3_RATIO_REF	
0x0069	25:24	R/W	OOF3_RATIO_REF	

Table 13.51. Register 0x0092 Fast LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x0092	0	R/W	LOL_FST_EN_PLLA	Fast LOL Enable. Large input frequency errors will quickly assert LOL when enabled. 0: Disable Fast LOL 1: Enable Fast LOL (default)
0x0092	1	R/W	LOL_FST_EN_PLLB	
0x0092	2	R/W	LOL_FST_EN_PLLC	
0x0092	3	R/W	LOL_FST_EN_PLLD	

Table 13.52. Register 0x0093-0x0094 Fast LOL Detection Window

Reg Address	Bit Field	Type	Name	Description
0x0093	3:0	R/W	LOL_FST_DETWIN_SEL_PLLA	Values calculated by CBPro.
0x0093	7:4	R/W	LOL_FST_DETWIN_SEL_PLLB	
0x0094	3:0	R/W	LOL_FST_DETWIN_SEL_PLLC	
0x0094	7:4	R/W	LOL_FST_DETWIN_SEL_PLLD	

Table 13.53. Register 0x0095 Fast LOL Detection Value

Reg Address	Bit Field	Type	Name	Description
0x0095	1:0	R/W	LOL_FST_VALWIN_SEL_PLLA	Values calculated by CBPro.
0x0095	3:2	R/W	LOL_FST_VALWIN_SEL_PLLB	
0x0095	5:4	R/W	LOL_FST_VALWIN_SEL_PLLC	
0x0095	7:6	R/W	LOL_FST_VALWIN_SEL_PLLD	

Table 13.54. Register 0x0096-0x0097 Fast LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0096	3:0	R/W	LOL_FST_SET_THR_SEL_PLLA	Values calculated by CBPro.
0x0096	7:4	R/W	LOL_FST_SET_THR_SEL_PLLB	
0x0097	3:0	R/W	LOL_FST_SET_THR_SEL_PLLC	
0x0097	7:4	R/W	LOL_FST_SET_THR_SEL_PLLD	

Table 13.55. Register 0x0098-0x0099 Fast LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0098	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLA	Values calculated by CBPro.
0x0098	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLB	
0x0099	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLC	
0x0099	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLD	

Table 13.56. Register 0x009A LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x009A	3:0	R/W	LOL_SLOW_EN_PLL[D:A]	Enable LOL detection. 0: LOL Disabled 1: LOL Enabled

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 13.57. Register 0x009B-0x009C Slow LOL Detection Value

Reg Address	Bit Field	Type	Name	Description
0x009B	3:0	R/W	LOL_SLW_DETWIN_SEL_PLLA	Values calculated by CBPro.
0x009B	7:4	R/W	LOL_SLW_DETWIN_SEL_PLLB	
0x009C	3:0	R/W	LOL_SLW_DETWIN_SEL_PLLC	
0x009C	7:4	R/W	LOL_SLW_DETWIN_SEL_PLLD	

Table 13.58. Register 0x009D Slow LOL Detection Window

Reg Address	Bit Field	Type	Name	Description
0x009D	1:0	R/W	LOL_SLW_VALWIN_SEL_PLLA	Values calculated by CBPro.
0x009D	3:2	R/W	LOL_SLW_VALWIN_SEL_PLLB	
0x009D	5:4	R/W	LOL_SLW_VALWIN_SEL_PLLC	
0x009D	7:6	R/W	LOL_SLW_VALWIN_SEL_PLLD	

Table 13.59. Register 0x009E LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x009E	3:0	R/W	LOL_SLW_SET_THR_PLLA	LOL Set Threshold. See the list below for settings.
0x009E	7:4	R/W	LOL_SLW_SET_THR_PLLB	
0x009F	3:0	R/W	LOL_SLW_SET_THR_PLLC	
0x009F	7:4	R/W	LOL_SLW_SET_THR_PLLD	

Table 13.60. Register 0x00A0 LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x00A0	3:0	R/W	LOL_SLW_CLR_THR_PLLA	LOL Clear Threshold. See the list below for settings.
0x00A0	7:4	R/W	LOL_SLW_CLR_THR_PLLB	
0x00A1	3:0	R/W	LOL_SLW_CLR_THR_PLLC	
0x00A1	7:4	R/W	LOL_SLW_CLR_THR_PLLD	

LOL_SET_THR and LOL_CLR_THR Threshold settings:

- 0 = ±0.1 ppm
- 1 = ±0.3 ppm

- 2 = ±1 ppm
- 3 = ±3 ppm
- 4 = ±10 ppm
- 5 = ±30 ppm
- 6 = ±100 ppm
- 7 = ±300 ppm
- 8 = ±1000 ppm
- 9 = ±3000 ppm
- 10 = ±10000 ppm
- 11 - 15 Reserved

Table 13.61. Register 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Name	Description
0x00A2	3:0	R/W	LOL_TIMER_EN_PLL[D:A]	Enable Delay for LOL Clear. 0: Disable Delay for LOL Clear 1: Enable Delay for LOL Clear

Extends the time after a clock returns or stabilizes before LOL de-asserts.

Table 13.62. Register 0x00A4-0x00B6 LOL Clear Delay

Reg Address	Bit Field	Type	Name	Description
0x00A4	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLA	29-bit value
0x00A5	15:8			
0x00A6	23:16			
0x00A7	28:24			
0x00A9	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLB	29-bit value
0x00AA	15:8			
0x00AB	23:16			
0x00AC	28:24			
0x00AE	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLC	29-bit value
0x00AF	15:8			
0x00B0	23:16			
0x00B1	28:24			
0x00B3	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLD	29-bit value
0x00B4	15:8			
0x00B5	23:16			
0x00B6	28:24			

Table 13.63. Register 0x00E2 NVM Active Bank

Reg Address	Bit Field	Type	Name	Description
0x00E2	7:0	R	ACTIVE_NVM_BANK	0x03 when no NVM has been burned 0x0F when 1 NVM bank has been burned 0x3F when 2 NVM banks have been burned When ACTIVE_NVM_BANK = 0x3F, the last bank has already been burned. See 2.1.2 NVM Programming for a detailed description of how to program the NVM.

Table 13.64. Register 0x00E3

Reg Address	Bit Field	Type	Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

See 2.1.2 NVM Programming.

Table 13.65. Register 0x00E4

Reg Address	Bit Field	Type	Name	Description
0x00E4	0	S	NVM_READ_BANK	Set to 1 to initiate NVM copy to registers.

Table 13.66. Register 0x00E5 Fastlock Extend Enable

Reg Address	Bit Field	Type	Name	Description
0x00E5	4	R/W	FASTLOCK_EXTEND_EN_PLLA	Enables FASTLOCK_EXTEND.
0x00E5	5	R/W	FASTLOCK_EXTEND_EN_PLLB	
0x00E5	6	R/W	FASTLOCK_EXTEND_EN_PLLC	
0x00E5	7	R/W	FASTLOCK_EXTEND_EN_PLLD	

Table 13.67. Register 0x00E6-0x00E9 FASTLOCK_EXTEND_PLLA

Reg Address	Bit Field	Type	Name	Description
0x00E6	7:0	R/W	FASTLOCK_EXTEND_PLLA	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00E7	15:8	R/W	FASTLOCK_EXTEND_PLLA	
0x00E8	23:16	R/W	FASTLOCK_EXTEND_PLLA	
0x00E9	28:24	R/W	FASTLOCK_EXTEND_PLLA	

Table 13.68. Register 0x00EA-0x00ED FASTLOCK_EXTEND_PLLB

Reg Address	Bit Field	Type	Name	Description
0x00EA	7:0	R/W	FSTLK_TIMER_EXT_PLLB	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00EB	15:8	R/W	FSTLK_TIMER_EXT_PLLB	
0x00EC	23:16	R/W	FSTLK_TIMER_EXT_PLLB	
0x00ED	28:24	R/W	FSTLK_TIMER_EXT_PLLB	

Table 13.69. Register 0x00EE-0x00F1 FASTLOCK_EXTEND_PLLC

Reg Address	Bit Field	Type	Name	Description
0x00EE	7:0	R/W	FASTLOCK_EXTEND_PLLC	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00EF	15:8	R/W	FASTLOCK_EXTEND_PLLC	
0x0060	23:16	R/W	FASTLOCK_EXTEND_PLLC	
0x0061	28:24	R/W	FASTLOCK_EXTEND_PLLC	

Table 13.70. Register 0x00F2-0x00F5 FASTLOCK_EXTEND_PLLD

Reg Address	Bit Field	Type	Name	Description
0x00F2	7:0	R/W	FASTLOCK_EXTEND_PLLD	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00F3	15:8	R/W	FASTLOCK_EXTEND_PLLD	
0x00F4	23:16	R/W	FASTLOCK_EXTEND_PLLD	
0x00F5	28:24	R/W	FASTLOCK_EXTEND_PLLD	

Table 13.71. Register 0x00FE Device Ready

Reg Address	Bit Field	Type	Name	Description
0x00FE	7:0	R	DEVICE_READY	Device Ready indicator. 0x0F: Device is Ready 0xF3: Device is Not ready

Read-only byte to indicate when the device is ready to accept serial bus writes. The user can poll this byte starting at power-up. When reads from DEVICE_READY return 0x0F the user can safely read or write to all registers. Generally, this is only needed after POR, Hard Reset, or after initiating an NVM write. This “Device Ready” register is available on every page in the device at the second to the last serial address, 0xFE. For example, there is a device ready register at 0x00FE, 0x01FE, 0x02FE, 0x03FE, etc. Since this register is accessible on every page, you should not write the page register when reading DEVICE_READY.

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Table 13.72. Register 0x0102 Global Output Gating for all Clock Outputs

Reg Address	Bit Field	Type	Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	Enable/Disable All output drivers. If the OEb pin is held high, then all outputs will be disabled regardless of this setting. 0: Disable All outputs (default) 1: Enable All outputs

Table 13.73. Register 0x0103 OUT0A Output Enable and R0A Divider Configuration

Reg Address	Bit Field	Type	Name	Description
0x0103	0	R/W	OUT0A_PDN	Powerdown output driver. 0: Normal Operation (default) 1: Powerdown output driver When powered down, outputs pins will be high impedance with a light pull down effect.
0x0103	1	R/W	OUT0A_OE	Enable/Disable individual output. 0: Disable output (default) 1: Enable output
0x0103	2	R/W	OUT0A_RDIV_FORCE	Force R0A output divider divide-by-2. 0: R0A_REG sets divide value (default) 1: Divide value forced to divide-by-2
0x0103	3	R/W	OUT0A_DIV2_BYP	Output divide-by-2 bypass. 0: Use output divide-by-2 (default) 1: Disable output divide-by-2

Setting R0A_REG=0 will not set the divide value to divide-by-2 automatically. OUT0A_RDIV_FORCE must be also be set to a value of 1 to force R0A to divide-by-2. Note that the R0A_REG value will be ignored while OUT0A_RDIV_FORCE=1. See R0A_REG registers, 0x0247-0x0249, for more information. Note that setting OUTx_DIV2_BYP = 1, the output clock duty cycle will be set by the N output divider value.

Table 13.74. Register 0x0104 OUT0A Output Format and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0104	2:0	R/W	OUT0A_FORMAT	Select output format. 0: Reserved 1: Differential Normal mode 2: Differential Low-Power mode 3: Reserved 4: LVCMOS single ended 5: LVCMOS (OUTx pin only) 6: LVCMOS (OUTxb pin only) 7: Reserved
0x0104	3	R/W	OUT0A_SYNC_EN	Synchronous Enable/Disable selection. 0: Asynchronous Enable/Disable (default) 1: Synchronous Enable/Disable (Glitchless)
0x0104	5:4	R/W	OUT0A_DIS_STATE	Determines the logic state of the output driver when disabled: 0: Disable logic Low 1: Disable logic High 2-3: Reserved
0x0104	7:6	R/W	OUT0A_CMOS_DRV	LVCMOS output impedance selection. See 4.6.2 LVCMOS Output Impedance and Drive Strength Selection for valid selections.

Table 13.75. Register 0x0105 Output OUT0A Differential Amplitude and Common Mode

Reg Address	Bit Field	Type	Name	Description
0x0105	3:0	R/W	OUT0A_CM	OUT0A Common Mode Voltage selection. Only applies when OUT0A_FORMAT=1 or 2.
0x0105	6:4	R/W	OUT0A_AMPL	OUT0A Differential Amplitude setting. Only applies when OUT0A_FORMAT=1 or 2.

ClockBuilder Pro is used to select the correct settings for this register. See Table 4.7 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML on page 45 and 15. Appendix—Custom Differential Amplitude Controls for details of the settings.

Table 13.76. Register 0x0106 Output OUT0A Source Selection and LVCMOS Inversion

Reg Address	Bit Field	Type	Name	Description
0x0106	2:0	R/W	OUT0A_MUX_SEL	OUT0A output source divider select. 0: DSPLL A is the source for OUT0A 1: DSPLLB/N1 is the source for OUT0A 2: DSPLL C is the source for OUT0A 3: DSPLL D is the source for OUT0A 4: DSPLLB/N4 is the source for OUT0A 5-7: Reserved
0x0106	3	R/W	OUT0A_VDD_SEL_EN	Output Driver VDD Select Enable. Set to 1 for normal operation.
0x0106	5:4	R/W	OUT0A_VDD_SEL	Output Driver VDD Select. 0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x0106	7:6	R/W	OUT0A_INV	OUT0A output LVCMOS inversion. Only applies when OUT0A_FORMAT = 4. See 4.6.4 LVCMOS Output Polarity for more information.

The OUTx_MUX_SEL settings should match the corresponding OUTx_DIS_SRC selections. Note that the setting codes for OUTx_DIS_SRC and OUTx_MUX_SEL are different when selecting the same DSPLL and N-divider.

All output drivers are identical in terms of control. The single set of descriptions above for OUT0A also applies to OUT0-OUT9A:

Table 13.77. Register 0x0107 Output Disable Source DSPLL

Reg Address	Bit Field	Type	Name	Description
0x0107	2:0	R/W	OUT0A_DIS_SRC	Output clock Squelched (temporary disable) on DSPLL Soft Reset: 0: Reserved 1: DSPLL A squelches output 2: DSPLL B squelches output 3: DSPLL C squelches output 4: DSPLL D squelches output 5-7: Reserved

The CLKx_DIS_SRC settings should match the corresponding OUTx_MUX_SEL selections. Note that the setting codes for OUTx_DIS_SRC and OUTx_MUX_SEL are different when selecting the same DSPLL.

Table 13.78. Output Registers Following the Same Definitions as OUT0A

Register Address	Description	(Same as) Address
0x0108	OUT0 Powerdown, Output Enable, and R0 Divide-by-2	0x0103
0x0109	OUT0 Signal Format and Configuration	0x0104
0x010A	OUT0 Differential Amplitude and Common Mode	0x0105
0x010B	OUT0 Source Selection and LVCMOS Inversion	0x0106
0x010C	OUT0 Disable Source	0x0107
0x010D	OUT1 Powerdown, Output Enable, and R1 Divide-by-2	0x0103
0x010E	OUT1 Signal Format and Configuration	0x0104
0x010F	OUT1 Differential Amplitude and Common Mode	0x0105
0x0110	OUT1 Source Selection and LVCMOS Inversion	0x0106
0x0111	OUT1 Disable Source	0x0107
0x0112	OUT2 Powerdown, Output Enable, and R2 Divide-by-2	0x0103
0x0113	OUT2 Signal Format and Configuration	0x0104
0x0114	OUT2 Differential Amplitude and Common Mode	0x0105
0x0115	OUT2 Source Selection and LVCMOS Inversion	0x0106
0x0116	OUT2 Disable Source	0x0107
0x0117	OUT3 Powerdown, Output Enable, and R3 Divide-by-2	0x0103
0x0118	OUT3 Signal Format and Configuration	0x0104
0x0119	OUT3 Differential Amplitude and Common Mode	0x0105
0x011A	OUT3 Source Selection and LVCMOS Inversion	0x0106
0x011B	OUT3 Disable Source	0x0107
0x011C	OUT4 Powerdown, Output Enable, and R4 Divide-by-2	0x0103
0x011D	OUT4 Signal Format and Configuration	0x0104
0x011E	OUT4 Differential Amplitude and Common Mode	0x0105
0x011F	OUT4 Source Selection and LVCMOS Inversion	0x0106
0x0120	OUT4 Disable Source	0x0107
0x0121	OUT5 Powerdown, Output Enable, and R5 Divide-by-2	0x0103
0x0122	OUT5 Signal Format and Configuration	0x0104
0x0123	OUT5 Differential Amplitude and Common Mode	0x0105
0x0124	OUT5 Source Selection and LVCMOS Inversion	0x0106
0x0125	OUT5 Disable Source	0x0107
0x0126	OUT6 Powerdown, Output Enable, and R6 Divide-by-2	0x0103
0x0127	OUT6 Signal Format and Configuration	0x0104
0x0128	OUT6 Differential Amplitude and Common Mode	0x0105
0x0129	OUT6 Source Selection and LVCMOS Inversion	0x0106
0x012A	OUT6 Disable Source	0x0107

Register Address	Description	(Same as) Address
0x012B	OUT7 Powerdown, Output Enable, and R7 Divide-by-2	0x0103
0x012C	OUT7 Signal Format and Configuration	0x0104
0x012D	OUT7 Differential Amplitude and Common Mode	0x0105
0x012E	OUT7 Source Selection and LVCMOS Inversion	0x0106
0x012F	OUT7 Disable Source	0x0107
0x0130	OUT8 Powerdown, Output Enable, and R8 Divide-by-2	0x0103
0x0131	OUT8 Signal Format and Configuration	0x0104
0x0132	OUT8 Differential Amplitude and Common Mode	0x0105
0x0133	OUT8 Source Selection and LVCMOS Inversion	0x0106
0x0134	OUT8 Disable Source	0x0107
0x0135	OUT9 Powerdown, Output Enable, and R9 Divide-by-2	0x0103
0x0136	OUT9 Signal Format and Configuration	0x0104
0x0137	OUT9 Differential Amplitude and Common Mode	0x0105
0x0138	OUT9 Source Selection and LVCMOS Inversion	0x0106
0x0139	OUT9 Disable Source	0x0107
0x013A	OUT9A Powerdown, Output Enable, and R9A Divide-by-2	0x0103
0x013B	OUT9A Signal Format and Configuration	0x0104
0x013C	OUT9A Differential Amplitude and Common Mode	0x0105
0x013D	OUT9A Source Selection and LVCMOS Inversion	0x0106
0x013E	OUT9A Disable Source	0x0107

Table 13.79. Register 0x013F-0x0140 Output Force Enable

Reg Address	Bit Field	Type	Name	Description
0x013F	7:0	R/W	OUTX_ALWAYS_ON	Force output driver to remain active, even when fault conditions are present. Used primarily for ZDM. 0: Normal output driver enable/disable (default) 1: Force driver always active (ZDM) [OUT6, OUT5, ..., OUT0, OUT0A]
0x0140	3:0	R/W	OUTX_ALWAYS_ON	[OUT9A, OUT9, OUT8, OUT7]

Table 13.80. Register 0x0141 Output Disable Mask for LOSXAXB

Reg Address	Bit Field	Type	Name	Description
0x0141	1	R/W	OUT_DIS_MSK	Mask alarms from disabling all output drivers. 0: Disable All output drivers on alarm (default) 1: Ignore alarms for output driver disable

Reg Address	Bit Field	Type	Name	Description
0x0141	6	R/W	OUT_DIS_LOSXAXB_MSK	Mask LOSXAXB from disabling all output drivers. 0: Disable All output drivers on LOSXAXB (default) 1: Ignore LOSXAXB for output driver disable

See 4.7.5 Output Driver Disable Source Summary for more information.

Table 13.81. Register 0x0142 Output Disable Mask for LOL

Reg Address	Bit Field	Type	Name	Description
0x0142	3:0	R/W	OUT_DIS_MASK_LOL_PLL[D:A]	Mask LOL from disabling all output drivers. 0: Disable All output drivers on LOL (default) 1: Ignore LOL for output driver disable

See 4.7.5 Output Driver Disable Source Summary for more information.

Table 13.82. Register 0x0145 Output Power Down All

Reg Address	Bit Field	Type	Name	Description
0x0145	0	R/W	OUT_PDN_ALL	Powerdown all output drivers. 0: Normal Operation (default) 1: Powerdown all output drivers

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Table 13.83. Register 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8			
0x020A	23:16			
0x020B	31:24			
0x020C	39:32			
0x020D	47:40			

Table 13.84. Register 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8			
0x0210	23:16			
0x0211	31:24			

The P input divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. The new register values for the P divider will not take effect until the appropriate Px_UPDATE strobe is set as described below.

Note: This ratio of (Px_NUM / Px_DEN) MUST also be an integer when used with DSPLL B.

Table 13.85. Registers that Follow the P0_NUM and P0_DEN Above

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x0226-0x022B	P3 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x022C-0x022F	P3 Divider Denominator	32-bit Integer Number	0x020E-0x0211

Table 13.86. Register 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Name	Description
0x0230	0	S	P0_UPDATE	Set these bits for IN3 - IN0 to 1 to latch in new P-divider values. A device Soft Reset (0x001C[0]=1) will also latch in the new values.
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

The Px_UPDATE bit must be asserted to update the internal P divider numerator and denominator values. These update bits are provided in a single register so that all of the P input dividers can be changed at the same time.

Table 13.87. Register P0 Factional Division Enable

Reg Address	Bit Field	Type	Name	Description
0x0231	3:0	R/W	P0_FRACN_MODE	P0 (IN0) input divider fractional mode. Must be set to 0xB for proper operation.
0x0231	4	R/W	P0_FRAC_EN	P0 (IN0) input divider fractional enable. 0: Integer-only division. 1: Fractional (or Integer) division.

Table 13.88. Register P1 Factional Division Enable

Reg Address	Bit Field	Type	Name	Description
0x0232	3:0	R/W	P1_FRACN_MODE	P1 (IN1) input divider fractional mode. Must be set to 0xB for proper operation.
0x0232	4	R/W	P1_FRAC_EN	P1 (IN1) input divider fractional enable. 0: Integer-only division. 1: Fractional (or Integer) division.

Table 13.89. Register P2 Factional Division Enable

Reg Address	Bit Field	Type	Name	Description
0x0233	3:0	R/W	P2_FRACN_MODE	P2 (IN2) input divider fractional mode. Must be set to 0xB for proper operation.
0x0233	4	R/W	P2_FRAC_EN	P2 (IN2) input divider fractional enable. 0: Integer-only division. 1: Fractional (or Integer) division.

Table 13.90. Register P3 Factional Division Enable

Reg Address	Bit Field	Type	Name	Description
0x0234	3:0	R/W	P3_FRACN_MODE	P3 (IN3) input divider fractional mode. Must be set to 0x0B for proper operation
0x0234	4	R/W	P3_FRAC_EN	P3 (IN3) input divider fractional enable. 0: Integer-only division. 1: Fractional (or Integer) division.

Table 13.91. Register 0x0235–0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number.
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	47:40	R/W	MXAXB_NUM	

Changing this register during operation may cause indefinite loss of lock unless the guidelines in Section 2.1.1 Updating Registers During Device Operation. Operation are followed. Either MXAXB_UPDATE or SOFT_RST must be set to cause these changes to take effect.

Table 13.92. Register 0x023B–0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number.
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

Changing this register during operation may cause indefinite loss of lock unless the guidelines in Section 2.1.1 Updating Registers During Device Operation. Operation are followed. Either MXAXB_UPDATE or SOFT_RST must be set to cause these changes to take effect.

Table 13.93. Register 0x023F MXAXB Update

Reg Address	Bit Field	Type	Name	Description
0x023F	1	S	MXAXB_UPDATE	Set to 1 to update the MXAXB_NUM and MXAXB_DEN values. A SOFT_RST may also be used to update these values.

Table 13.94. Register 0x0247-0x0249 R0A Divider

Reg Address	Bit Field	Type	Name	Description
0x0247	7:0	R/W	R0A_REG	24-bit integer final R0A divider selection. R Divisor = (R0A_REG + 1) x 2 However, note that setting R0A_REG = 0 will not set the output to divide-by-2. See notes below.
0x0248	15:8			
0x0249	23:16			

The final output R dividers are even-numbered dividers beginning with divide-by-2. While all other values follow the formula in the bit description above, divide-by-2 requires an extra bit to be set. For divide-by-2, also set OUT0_RDIV_FORCE=1. See the description for register bit 0x0103[2] in this register map.

The R0-R9A dividers follow the same format as the R0A divider description above.

Table 13.95. Registers that Follow the R0A_REG

Register Address	Description	Size	Same as Address
0x024A-0x024C	R0_REG	24-bit Integer Number	0x0247-0x0249
0x024D-0x024F	R1_REG	24-bit Integer Number	0x0247-0x0249
0x0250-0x0252	R2_REG	24-bit Integer Number	0x0247-0x0249
0x0253-0x0255	R3_REG	24-bit Integer Number	0x0247-0x0249
0x0256-0x0258	R4_REG	24-bit Integer Number	0x0247-0x0249
0x0259-0x025B	R5_REG	24-bit Integer Number	0x0247-0x0249
0x025C-0x025E	R6_REG	24-bit Integer Number	0x0247-0x0249
0x025F-0x0261	R7_REG	24-bit Integer Number	0x0247-0x0249
0x0262-0x0264	R8_REG	24-bit Integer Number	0x0247-0x0249
0x0265-0x0267	R9_REG	24-bit Integer Number	0x0247-0x0249
0x0268-0x026A	R9A_REG	24-bit Integer Number	0x0247-0x0249

Table 13.96. Register 0x026B-0x0272 User Design Identifier

Reg Address	Bit Field	Type	Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by the ClockBuilder Pro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, "ULT. 1A" with null character padding sets: • DESIGN_ID0: 0x55 • DESIGN_ID1: 0x4C • DESIGN_ID3: 0x2E • DESIGN_ID4: 0x31 • DESIGN_ID5: 0x41 • DESIGN_ID6: 0x00 • DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 13.97. Register 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: Si5381A-E12346-GM, 12346 is the OPN unique identifier, which sets: • OPN_ID0: 0x31 • OPN_ID1: 0x32 • OPN_ID2: 0x33 • OPN_ID3: 0x34 • OPN_ID4: 0x36
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

See 12.3 Part Numbering Summary for more information on part numbers.

Table 13.98. Registers 0x028A - 0x028D OOFx_TRG_THR_EXT Controls

Reg Address	Bit Field	Type	Name	Description
0x028A	4:0	R/W	OOF0_TRG_THR_EXT	Set by CBPro.
0x028B	4:0	R/W	OOF1_TRG_THR_EXT	Set by CBPro.
0x028C	4:0	R/W	OOF2_TRG_THR_EXT	Set by CBPro.
0x028D	4:0	R/W	OOF3_TRG_THR_EXT	Set by CBPro.

Table 13.99. Registers 0x028E - 0x0291 OOFx_CLR_THR_EXT Controls

Reg Address	Bit Field	Type	Name	Description
0x028E	4:0	R/W	OOF0_CLR_THR_EXT	Set by CBPro.
0x028F	4:0	R/W	OOF1_CLR_THR_EXT	Set by CBPro.
0x0290	4:0	R/W	OOF2_CLR_THR_EXT	Set by CBPro.
0x0291	4:0	R/W	OOF3_CLR_THR_EXT	Set by CBPro.

Table 13.100. Register 0x0292 OOF Stop on LOS Controls

Reg Address	Bit Field	Type	Name	Description
0x0292	3:0	R/W	OOF_STOP_ON_LOS	Values set by CBPro.

Table 13.101. Register 0x0293 OOF Clear on LOS Controls

Reg Address	Bit Field	Type	Name	Description
0x0293	3:0	R/W	OOF_CLEAR_ON_LOS	Values set by CBPro.

Table 13.102. Register 0x0294-0x0295 Fastlock Extend Scale

Reg Address	Bit Field	Type	Name	Description
0x0294	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLA	Scales LOLB_INT_TIMER_DIV256. Set by CBPro.
0x0294	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLB	
0x0295	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLC	
0x0295	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLD	

Table 13.103. Register 0x0296 Fastlock Delay on Input Switch

Reg Address	Bit Field	Type	Name	Description
0x0296	0	R/W	LOL_SLW_VAL-WIN_SELX_PLLA	Set by CBPro.
0x0296	1	R/W	LOL_SLW_VAL-WIN_SELX_PLLB	
0x0296	2	R/W	LOL_SLW_VAL-WIN_SELX_PLLC	
0x0296	3	R/W	LOL_SLW_VAL-WIN_SELX_PLLD	

Table 13.104. Register 0x0297 Fastlock Delay on Input Switch

Reg Address	Bit Field	Type	Name	Description
0x0297	0	R/W	FAST-LOCK_DLY_ONSW_EN_PLLA	Set by CBPro.
0x0297	1	R/W	FAST-LOCK_DLY_ONSW_EN_PLLB	
0x0297	2	R/W	FAST-LOCK_DLY_ONSW_EN_PLLC	
0x0297	3	R/W	FAST-LOCK_DLY_ONSW_EN_PLLD	

Table 13.105. Register 0x0299 Fastlock Delay on LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x0299	0	R/W	FASTLOCK_DLY_ON-LOL_EN_PLLA	Set by CBPro.
0x0299	1	R/W	FASTLOCK_DLY_ON-LOL_EN_PLLB	
0x0299	2	R/W	FASTLOCK_DLY_ON-LOL_EN_PLLC	
0x0299	3	R/W	FASTLOCK_DLY_ON-LOL_EN_PLLD	

Table 13.106. Register 0x029A–0x029C Fastlock Delay on LOLA

Reg Address	Bit Field	Type	Name	Description
0x029A	7:0	R/W	FASTLOCK_DLY_ON-LOL_PLLA	Set by CBPro.
0x029B	15:8	R/W	FASTLOCK_DLY_ON-LOL_PLLA	
0x029C	19:16	R/W	FASTLOCK_DLY_ON-LOL_PLLA	

Table 13.107. Register 0x029D–0x029F Fastlock Delay on LOLB

Reg Address	Bit Field	Type	Name	Description
0x029D	7:0	R/W	FASTLOCK_DLY_ON-LOL_PLLB	Set by CBPro.
0x029E	15:8	R/W	FASTLOCK_DLY_ON-LOL_PLLB	
0x029F	19:16	R/W	FASTLOCK_DLY_ON-LOL_PLLB	

Table 13.108. Register 0x02A0–0x02A2 Fastlock Delay on LOLC

Reg Address	Bit Field	Type	Name	Description
0x02A0	7:0	R/W	FASTLOCK_DLY_ON-LOL_PLLC	Set by CBPro.
0x02A1	15:8	R/W	FASTLOCK_DLY_ON-LOL_PLLC	
0x02A2	19:16	R/W	FASTLOCK_DLY_ON-LOL_PLLC	

Table 13.109. Register 0x02A3–0x02A5 Fastlock Delay on LOLD

Reg Address	Bit Field	Type	Name	Description
0x02A3	7:0	R/W	FASTLOCK_DLY_ON-LOL_PLLD	Set by CBPro.
0x02A4	15:8	R/W	FASTLOCK_DLY_ON-LOL_PLLD	
0x02A5	19:16	R/W	FASTLOCK_DLY_ON-LOL_PLLD	

Table 13.110. Register 0x02A6–0x02A8 Fastlock Delay on Input Switch PLLA

Reg Address	Bit Field	Type	Name	Description
0x02A6	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLA	20-bit value. Set by CBPro.
0x02A7	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLA	
0x02A8	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLA	

Table 13.111. Register 0x02A9–0x02AB Fastlock Delay on Input Switch PLLB

Reg Address	Bit Field	Type	Name	Description
0x02A9	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLB	20-bit value. Set by CBPro.
0x02AA	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLB	
0x02AB	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLB	

Table 13.112. Register 0x02AC–0x02AE Fastlock Delay on Input Switch PLLC

Reg Address	Bit Field	Type	Name	Description
0x02AC	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLC	20-bit value. Set by CBPro.
0x02AD	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLC	
0x02AE	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLC	

Table 13.113. Register 0x02AF–0x02B1 Fastlock Delay on Input Switch PLLD

Reg Address	Bit Field	Type	Name	Description
0x02AF	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLD	20-bit value. Set by CBPro.
0x02B0	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLD	
0x02B1	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLD	

Table 13.114. Register 0x02B7 LOL Delay from LOS

Reg Address	Bit Field	Type	Name	Description
0x02B7	1:0	R/W	LOL_NO-SIG_TIME_PLLA	Set by CBPro.
0x02B7	3:2	R/W	LOL_NO-SIG_TIME_PLLB	
0x02B7	5:4	R/W	LOL_NO-SIG_TIME_PLLC	
0x02B7	7:6	R/W	LOL_NO-SIG_TIME_PLLD	

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Table 13.115. Register 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Name	Description
0x0302	7:0	R/W	N0_NUM	N Output Divider Numerator. 44-bit Integer
0x0303	15:8			
0x0304	23:16			
0x0305	31:24			
0x0306	39:32			
0x0307	43:40			

Table 13.116. Register 0x0308-0x030B N0 Denominator

Reg Address	Bit Field	Type	Name	Description
0x0308	7:0	R/W	N0_DEN	N Output Divider Denominator. 32-bit Integer
0x0309	15:8			
0x030A	23:16			
0x030B	31:24			

The N output divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. Note that this ratio of Nx_NUM / Nx_DEN should also be an integer for best performance. The N output dividers feed into the final output R dividers through the output crosspoint.

Table 13.117. Register 0x030C N0 Update

Reg Address	Bit Field	Type	Name	Description
0x030C	0	S	N0_UPDATE	Set this bit to 1 to latch the N output divider registers into operation.

Setting this self-clearing bit to 1 latches the new N output divider register values into operation. An individual or device Soft Reset will have the same effect.

Table 13.118. Registers that Follow the N0_NUM and N0_DEN Definitions

Register Address	Description	Size	Same as Address
0x030D-0x0312	N1_NUM	44-bit Integer	0x0302-0x0307
0x0313-0x0316	N1_DEN	32-bit Integer	0x0308-0x030B
0x0317	N1_UPDATE	one bit	0x030C
0x0318-0x031D	N2_NUM	44-bit Integer	0x0302-0x0307
0x031E-0x0321	N2_DEN	32-bit Integer	0x0308-0x030B
0x0322	N2_UPDATE	one bit	0x030C
0x0323-0x0328	N3_NUM	44-bit Integer	0x0302-0x0307
0x0329-0x032C	N3_DEN	32-bit Integer	0x0308-0x030B
0x032D	N3_UPDATE	one bit	0x030C

Register Address	Description	Size	Same as Address
0x032E-0x0333	N4_NUM	44-bit Integer	0x0302-0x0307
0x0334-0x0337	N4_DEN	32-bit Integer	0x0308-0x030B
0x0338	N4_UPDATE	one bit	0x030C

Table 13.119. Register 0x0338 Global N Divider Update

Reg Address	Bit Field	Type	Name	Description
0x0338	1	S	N_UPDATE_ALL	Writing a 1 to this bit will update the N output divider values. When this bit is written to 1, all other bits in this register must be written as zeros.

This bit is provided so that all of the N divider values can be changed at the same time. First, write all of the new values to Nx_NUM and Nx_DEN, then set the update bit to 1.

Note: If the intent is to write to the N_UPDATE_ALL to have all Nx dividers update at the same time then make sure only bit 1 N_UPDATE_ALL bit gets set in this register.

Table 13.120. Register 0x0339 DCO FINC/FDEC Control Mask

Reg Address	Bit Field	Type	Name	Description
0x0339	0	R/W	N_FSTEP_MSK_PLLA	DSPLL A DCO control mask. 0: Enable FINC/FDEC updates (default) 1: Disable FINC/FDEC updates

Table 13.121. Register 0x033B-0x0340 DCO Step Size for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x033B	7:0	R/W	N0_FSTEPW	44-bit Integer Number.
0x033C	15:8	R/W	N0_FSTEPW	
0x033D	23:16	R/W	N0_FSTEPW	
0x033E	31:24	R/W	N0_FSTEPW	
0x033F	39:32	R/W	N0_FSTEPW	
0x0340	43:40	R/W	N0_FSTEPW	

Table 13.122. Register 0x0347-0x034C DCO Step Size for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0347	7:0	R/W	N2_FSTEPW	44-bit Integer Number.
0x0348	15:8	R/W	N2_FSTEPW	
0x0349	23:16	R/W	N2_FSTEPW	
0x034A	31:24	R/W	N2_FSTEPW	
0x034B	39:32	R/W	N2_FSTEPW	
0x034C	43:40	R/W	N2_FSTEPW	

Table 13.123. Register 0x034D-0x0352 DCO Step Size for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x034D	7:0	R/W	N3_FSTEPW	44-bit Integer Number.
0x034E	15:8	R/W	N3_FSTEPW	
0x034F	23:16	R/W	N3_FSTEPW	
0x0350	31:24	R/W	N3_FSTEPW	
0x0351	39:32	R/W	N3_FSTEPW	
0x0352	43:40	R/W	N3_FSTEPW	

Table 13.124. Register 0x035B-0x035C N1 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035B-0x035C	7:0	R/W	N1_DELAY[15:8]	8.8-bit, 2s-complement delay for N1

N1_DELAY[7:0] is an 8.8-bit 2's-complement number that sets the output delay of the N1 divider. ClockBuilder Pro calculates the correct value for this register. A Soft Reset of the device, SOFT_RST (0x001C[0] = 1), required to latch in the new delay value(s). Note that the least significant byte (0x035B) is ignored when the N1 divider is in integer mode.

t_{DLY} = Nx_DELAY / 256 x 67.8 ps

f_{VCO}=14.7456 GHz, 1/f_{VCO}=67.8 ps

Table 13.125. Register 0x0361-0x0362 N4 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0361-0x0362	7:0	R/W	N4_DELAY[15:8]	8.8-bit, 2s-complement delay for N4

N4_DELAY behaves in the same manner as N1_DELAY above.

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Table 13.126. Register 0x0407 Input Selection for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0407	7:6	R	IN_ACTV_PLLA	Currently selected DSPLL A input clock. 0: IN0 1: IN1 2: IN2 3: IN3

This register displays the currently selected input for the DSPLL. In manual select mode, this reflects either the register value or the voltages on the IN_SEL1 and IN_SEL0 pins. In automatic switching mode, it reflects the input currently chosen by the automatic algorithm. If there are no valid input clocks in the automatic mode, this value will retain its previous value until a valid input clock is presented. Note that this value is not meaningful in Holdover or Freerun modes.

Table 13.127. Register 0x0408-0x040D DSPLL Loop Bandwidth for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0408	7:0	R/W	BW0_PLLA	DSPLL A loop bandwidth parameters.
0x0409	7:0	R/W	BW1_PLLA	
0x040A	7:0	R/W	BW2_PLLA	
0x040B	7:0	R/W	BW3_PLLA	
0x040C	7:0	R/W	BW4_PLLA	
0x040D	7:0	R/W	BW5_PLLA	

This group of registers determines the DSPLL A loop bandwidth. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that individual SOFT_RST_PLLA (0x001C[1]) does not update the bandwidth parameters.

Table 13.128. Register 0x040E-0x0413 DSPLL Fastlock Loop Bandwidth for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x040E	7:0	R/W	FAST-LOCK_BW0_PLLA	DSPLL A Fastlock Bandwidth parameters.
0x040F	7:0	R/W	FAST-LOCK_BW1_PLLA	
0x0410	7:0	R/W	FAST-LOCK_BW2_PLLA	
0x0411	7:0	R/W	FAST-LOCK_BW3_PLLA	
0x0412	7:0	R/W	FAST-LOCK_BW4_PLLA	
0x0413	7:0	R/W	FAST-LOCK_BW5_PLLA	

This group of registers determines the DSPLL Fastlock bandwidth. In ClockBuilder Pro, it is selectable from 200 Hz to 4 kHz in factors of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that individual SOFT_RST_PLLA (0x001C[1]) does not update the bandwidth parameters.

Table 13.129. Register 0x0414 DSPLL Bandwidth Update for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0414	0	S	BW_UPDATE_PLLA	Set to 1 to latch updated BWx_PLLA and FAST_BWx_PLLA bandwidth registers into operation.

Setting this self-clearing bit high latches all of the new DSPLL A bandwidth register values into operation. Asserting this strobe will update all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA bandwidths at the same time. A device Soft Reset (0x001C[0]) will have the same effect, but individual DSPLL soft resets will not update these values.

Table 13.130. Register 0x0415-0x041B M Feedback Divider Numerator, 56-bits for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0415	7:0	R/W	M_NUM_PLLA	M feedback divider Numerator 56-bit Integer
0x0416	15:8			
0x0417	23:16			
0x0418	31:24			
0x0419	39:32			
0x041A	47:40			
0x041B	55:48			

Table 13.131. Register 0x041C-0x041F M Feedback Divider Denominator, 32-bits for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x041C	7:0	R/W	M_DEN_PLLA	M feedback divider Denominator 32-bit Integer
0x041D	15:8			
0x041E	23:16			
0x041F	31:24			

The DSPLL M feedback divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. An Integer ratio of (M_NUM / M_DEN) will give the best phase noise performance.

Table 13.132. Register 0x0420 M Divider Update for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0420	0	S	M_UPDATE_PLLA	Set this bit to latch the M feedback divider register values into operation.

Setting this self-clearing bit high latches the new M feedback divider register values into operation. A Soft Reset will have the same effect.

Table 13.133. Register 0x0421 A M Divider Fractional Enable for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0421	3:0	R/W	M_FRAC_MODE_PLLA	M feedback divider fractional mode. Must be set to 0xB for proper operation
0x0421	4	R/W	M_FRAC_EN_PLLA	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0421	5	R/W	Reserved	Must be set to 1 for DSPLL A

Table 13.134. Register 0x0422 A M Divider DSO Step Mask for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0422	0	R/W	M_FSTEPW_MASK_PLLA	M feedback divider DCO mask 0: Enable FINC/FDEC Updates (default) 1: Disable FINC/FDEC Updates

Table 13.135. Register 0x0423-0x0429 M Divider DCO FSTEPW for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0423	7:0	R/W	M_FSTEPW_PLLA	56-bit number
0x0424	15:8			
0x0425	23:16			
0x0426	31:24			
0x0427	39:32			
0x0428	47:40			
0x0429	55:48			

Table 13.136. Register 0x042A Input Clock Select for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x042A	2:0	R/W	IN_SEL_PLLA	Manual Input Select selection (Non-ZDM). 0: IN0 (default), 1: IN1, 2: IN2, 3: IN3 4-7: Reserved

Input clock selection for manual register based and pin controlled clock selection.

Note: When IN_SEL_REGCTRL is low, IN_SEL does not do anything and the clock selection is pin controlled.

Table 13.137. Register 0x042B Fastlock Control for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x042B	0	R/W	FASTLOCK_AUTO_EN_PLLA	Auto Fastlock Enable/Disable. 0: Disable Auto Fastlock (default) 1: Enable Auto Fastlock
0x042B	1	R/W	FASTLOCK_MAN_PLLA	Manually Force Fastlock. 0: Normal Operation (default) 1: Force Fastlock

When Fastlock is enabled by either manual or automatic means, the higher Fastlock bandwidth will be used to provide faster settling of the DSPLL. With FASTLOCK_MAN_PLLA=0 and FASTLOCK_AUTO_EN_PLLA=1, the DSPLL will automatically revert to the loop bandwidth when the loop has locked and LOL deasserts. See 1.4.1 Fastlock for more information on Fastlock behavior.

Table 13.138. Register 0x042C Holdover Exit Control for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x042C	0	R/W	HOLD_EN_PLLA	Holdover enable 0: Holdover Disabled 1: Holdover Enabled (default)
0x042C	3	R/W	HOLD_RAMP_BYP_PLLA	Must be set to 1 for Normal Operation.
0x042C	4	R/W	HOLD_EXITBW_SEL_PLLA	Selects the exit rate from Holdover bandwidth 0: Exit Holdover using Fastlock bandwidth (default) 1: Exit Holdover using the DSPLL loop bandwidth
0x042C	7:5	R/W	HOLD_RAMP_RATE_PLLA	Sets the base rate for ramped input switching and Holdover Entry/Exit. This value is multiplied by the RAMP_STEP_ADJ_PLLA factor to find the ramp rate. 0: 1.48 ppm/s 1: 2.22 ppm/s 2: 2.53 ppm/s 3: 1.18 ppm/s 4: 0.74 ppm/s 5: 5.06 ppm/s 6: 10.12 ppm/s 7: 40.48 ppm/s Ramp Rate = HOLD_RAMP_RATE_PLLA * RAMP_STEP_ADJ_PLLA

When a valid input is presented to the DSPLL while the device is in Holdover or Freerun mode, the higher Fastlock bandwidth can be enabled to provide faster DSPLL settling. When a slower response is desired, then the regular loop bandwidth may be used instead.

Table 13.139. Register 0x042E Holdover History Average Length for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x042E	4:0	R/W	HOLD_HIST_LEN_PLLA	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds: Window Length = $(2^{HOLD\_HIST\_LEN\_PLLA} - 1) \times 8 / 3 \times 10^{-7}$

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See 2.5 Holdover Mode to calculate the window length from the register value.

Table 13.140. Register 0x042F Holdover History Delay for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x042F	4:0	R/W	HOLD_HIST_DELAY_PLLA	Delay Time to ignore data at the end of the historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $2^{HOLD\_HIST\_DELAY\_PLLA} \times 2 / 3 \times 10^{-7}$

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See 2.5 Holdover Mode to calculate the ignore delay time from the register value.

Table 13.141. Register 0x0432-0x0424 Holdover Cycle Count DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0432	7:0	R/W	HOLD_15M_CYC_COUNT_PLLA	Value calculated in CBPro.
0x0433	15:8	R/W	HOLD_15M_CYC_COUNT_PLLA	
0x0434	23:16	R/W	HOLD_15M_CYC_COUNT_PLLA	

Table 13.142. Register 0x0435 Force Holdover for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0435	0	R/W	FORCE_HOLD_PLLA	Force the device into Holdover mode. Used to hold the device output clocks while retraining an upstream input clock. 0: Normal Operation 1: Force Holdover/Freerun Mode: HOLD_HIST_VALID_PLLA = 0 => Freerun Mode HOLD_HIST_VALID_PLLA = 1 => Holdover Mode

Table 13.143. Register 0x0436 Input Clock Switching Control for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0436	1:0	R/W	CLK_SWITCH_MODE_PLLA	Selects manual or automatic switching modes. Automatic mode can be Revertive or Non-revertive. 0: Manual (default) 1: Automatic Non-revertive 2: Automatic Revertive 3: Reserved
0x0436	2	R/W	HSW_EN_PLLA	Enable Hitless Switching. 0: Disable Hitless switching (default) 1: Enable Hitless switching (phase buildout enabled)

Table 13.144. Register 0x0437 Input Fault Masks for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0437	3:0	R/W	IN_LOS_MSK_PLLA	Enables the use of IN3 - IN0 LOS status in determining a valid clock for automatic input selection. 0: Use LOS in automatic clock switching logic (default) 1: Mask (ignore) LOS from automatic clock switching logic

Reg Address	Bit Field	Type	Name	Description
0x0437	7:4	R/W	IN_OOF_MSK_PLLA	Determines the OOF status for IN3 - IN0 and is used in determining a valid clock for the automatic input selection. 0: Use OOF in the automatic clock switching logic (default) 1: Mask (ignore) OOF from automatic clock switching logic

This register is for the input clock fault masks. For each of the four clock inputs, the OOF and/or the LOS fault can be used for the clock selection logic or they can be masked from it.

Note: The clock selection logic can affect entry into Holdover.

Table 13.145. Register 0x0438-0x0439 Clock Input Priorities for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0438	2:0	R/W	IN0_PRIORITY_PLLA	IN0 - IN3 priority assignment for the automatic switching state machine. Priority assignments in descending importance are: 1, 2, 3, 4 (or 0 for never select) 5-7: Reserved
0x0438	6:4	R/W	IN1_PRIORITY_PLLA	
0x0439	2:0	R/W	IN2_PRIORITY_PLLA	
0x0439	6:4	R/W	IN3_PRIORITY_PLLA	

This register is used to assign priority to each input clock for automatic clock input switching. The available clock with the highest priority will be selected. Priority 1 is first and most likely to be selected, followed by priorities 2-4. Priority 0 prevents the clock input from being automatically selected, though it may still be manually selected. When two valid input clocks are assigned the same priority, the lowest numbered input will be selected. In other words, IN0 has priority over IN1-IN3, IN1 has priority over IN2-IN3, etc, when the priorities are the same.

Table 13.146. Register 0x043A Hitless Switching Mode DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x043A	1:0	R/W	HSW_MODE_PLLA	1: Default setting, do not modify 0, 2, 3: Reserved
0x043A	3:2	R/W	HSW_PHMEAS_CTRL_PLLA	0: Default setting, do not modify 1, 2, 3: Reserved

Table 13.147. Register 0x043B–0x044C Hitless Switching Phase Threshold DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x043B	7:0	R/W	HSW_PHMEAS_THR_PLLA	Value calculated in CBPro.
0x043C	9:8	R/W	HSW_PHMEAS_THR_PLLA	

Table 13.148. Register 0x043D Hitless Switching Length DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x043D	4:0	R/W	HSW_COARSE_PM_LEN_PLLA	Value calculated in CBPro.

Table 13.149. Register 0x043E Hitless Switching Length DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x043E	4:0	R/W	HSW_COARSE_PM_DLY_PLLA	Value calculated in CBPro.

Table 13.150. Register 0x043F DSPLL Hold Valid and Fastlock Status for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x043F	1	R	HOLD_HIST_VALID_PLLA	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x043F	2	R	FASTLOCK_STATUS_PLLA	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLA accumulation will stop. When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 13.151. Register 0x0487 Zero Delay Mode Setup for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0487	0	R/W	ZDM_EN	Enable ZDM Operation. 0: Disable Zero Delay Mode (default) 1: Enable Zero Delay Mode
0x0487	2:1	R/W	ZDM_IN_SEL	ZDM Manual Input Source Select. 0: IN0 (default) 1: IN1 2: IN2 3: Reserved (IN3 already used by ZDM)

To enable ZDM, set ZDM_EN = 1. In ZDM, the input clock source must be selected manually by using either the ZDM_IN_SEL register bits or the IN_SEL1 and IN_SEL0 device input pins. IN_SEL_REGCTRL determiens the choice of register or pin control to select the desired input clock. When register control is selected in ZDM, the ZDM_IN_SEL control bits determine the input to be used and the non-ZDM IN_SEL bits will be ignored. Note that in ZDM, the DSPLL does not use either Hitless switching or Automatic input source switching.

Table 13.152. Register 0x0487 Zero Delay Mode Setup for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0487	0	R/W	ZDM_EN	Enable ZDM Operation for DSPLL A. 0: Disable Zero Delay Mode (default) 1: Enable Zero Delay Mode
0x0487	2:1	R/W	ZDM_IN_SEL	ZDM Manual Input Source Select for DSPLL A when both ZDM_EN = 1 and IN_SEL_REGCTRL (0x052A[0]) = 1. 0: IN0 (default) 1: IN1 2: IN2 3: Reserved (IN3 already used by ZDM)

To enable ZDM, set ZDM_EN = 1. In ZDM, the input clock source must be selected manually by using either the ZDM_IN_SEL register bits or the IN_SEL1 and IN_SEL0 device input pins. IN_SEL_REGCTRL determines the choice of register or pin control to select the desired input clock. When register control is selected in ZDM, the ZDM_IN_SEL control bits determine the input to be used and the non-ZDM IN_SEL bits will be ignored. Note that in ZDM, the DSPLL does not use either Hitless switching or Automatic input source switching.

Table 13.153. Register 0x0488 Fine Hitless Switching PM Length for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0488	3:0	R/W	HSW_FINE_PM_LEN_PLLA	Values set by CBPro.

Table 13.154. Register 0x0489 - 0x049A PFD Enable Delay for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0489	7:0	R/W	PFD_EN_DELAY_PLLA	Set by CBPro.
0x048A	12:8	R/W	PFD_EN_DELAY_PLLA	

Table 13.155. Register 0x049B Holdover Exit for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x049B	1	R/W	INIT_LP_CLOSE_HO_PLLA	PLL acquisition method for Freerun to Lock transition. 0: Normal loop closure 1: Holdover exit ramp (default)

Reg Address	Bit Field	Type	Name	Description
0x049B	4	R/W	HOLD_PRE-SERVE_HIST_PLLA	Preserve Holdover history when the input clock is lost or switched. 0: Clear Holdover history when the input clock is lost or switched. 1: Preserve Holdover history when the input clock is lost or switched. (default)
0x049B	5	R/W	HOLD_FRZ_WITH_IN TONLY_PLLA	Holdover Freeze control when the input clock is lost or switched. 0: Use filter output on Freeze. 1: Use Integrator-only on Freeze. (default)
0x049B	6	R/W	HOLDEX-IT_BW_SEL0_PLLA	Set by CBPro.
0x049B	7	R/W	HOLDEX-IT_STD_BO_PLLA	1: Default setting, do not modify 0: Reserved

Table 13.156. Register 0x049C Holdover Exit Control for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x049C	6	R/W	HOLDEX-IT_ST_BO_PLLA	Value set by CBPro.
0x049C	7	R/W	HOLD_RAMPBP_NO HIST_PLLA	Value set by CBPro.

Table 13.157. Register 0x049D-0x04A2 Holdover Exit Bandwidth for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x049D	7:0	R/W	HOLDEX-IT_BW0_PLLA	DSPLL A Holdover Exit bandwidth parameters calculated by CBPro when ramp switching is disabled.
0x049E	7:0	R/W	HOLDEX-IT_BW1_PLLA	
0x049F	7:0	R/W	HOLDEX-IT_BW2_PLLA	
0x04A0	7:0	R/W	HOLDEX-IT_BW3_PLLA	
0x04A1	7:0	R/W	HOLDEX-IT_BW4_PLLA	
0x04A2	7:0	R/W	HOLDEX-IT_BW5_PLLA	

This group of registers determines the DSPLL A bandwidth used when exiting Holdover Mode. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that the individual SOFT_RST_PLLA (0x001C[1]) does not update these bandwidth parameters.

Table 13.158. Register 0x04A4 Hitless Switching Limit for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04A4	7:0	R/W	HSW_LIMIT_PLLA	Value set by CBPro.

Table 13.159. Register 0x04A5 Hitless Switching Limit Action for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04A5	0	R/W	HSW_LIMIT_AC-TION_PLLA	Value set by CBPro.

Table 13.160. Register 0x04A6 Hitless Switching Ramp Control for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04A6	2:0	R/W	RAMP_STEP_ADJ_PLLA	Scaling factor for ramped input switching and Holdover Entry/Exit. Multiply with HOLD_RAMP_RATE_PLLA to calculate final ramp rate. 0: 1x 1: 4x 2: 16x 3: 64x 4: 256x 5: 1024x 6: 1/4x 7: 1/2x Ramp Rate = HOLD_RAMP_RATE_PLLA * RAMP_STEP_ADJ_PLLA
0x04A6	3	R/W	RAMP_SWITCH_EN_PLLA	Enable ramped input switching and entry into Holdover/Freerun. 0: Disable ramped input switching and entry into Holdover 1: Enable ramped input switching and entry into Holdover

Table 13.161. Register 0x04AC Configuration for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04AC	0	R/W	OUT_MAX_LIM-IT_EN_PLLA	Set by CBPro.
0x04AC	3	R/W	HOLD_SET-TLE_DET_EN_PLLA	Set by CBPro.

Table 13.162. Register 0x04AD - 0x04AE Configuration for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04AD	7:0	R/W	OUT_MAX_LIM-IT_LMT_PLLA	Set by CBPro.
0x04AE	15:0	R/W		

Table 13.163. Register 0x04B1 - 0x04B2 Configuration for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04B1	7:0	R/W	HOLD_SETTLE_TAR-GET_PLLA	Set by CBPro.
0x04B2	15:0	R/W		

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Table 13.164. Register 0x0507 Input Selection for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0507	7:6	R	IN_ACTV_PLLB	Currently selected DSPLL B input clock. 0: IN0 1: IN1 2: IN2 3: IN3

This register displays the currently selected input for the DSPLL. In manual select mode, this reflects either the register value or the voltages on the IN_SEL1 and IN_SEL0 pins. In automatic switching mode, it reflects the input currently chosen by the automatic algorithm. If there are no valid input clocks in the automatic mode, this value will retain its previous value until a valid input clock is presented. Note that this value is not meaningful in Holdover or Freerun modes.

Table 13.165. Register 0x0508-0x050D DSPLL Loop Bandwidth for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0508	7:0	R/W	BW0_PLLB	DSPLL B loop bandwidth parameters.
0x0509	7:0	R/W	BW1_PLLB	
0x050A	7:0	R/W	BW2_PLLB	
0x050B	7:0	R/W	BW3_PLLB	
0x050C	7:0	R/W	BW4_PLLB	
0x050D	7:0	R/W	BW5_PLLB	

This group of registers determines the DSPLL B loop bandwidth. In ClockBuilder Pro it is selectable from 10 Hz to 100 Hz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 13.166. Register 0x050E-0x0513 DSPLL Fastlock Loop Bandwidth for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x050E	7:0	R/W	FAST_BW0_PLLB	DSPLL B Fastlock Bandwidth parameters.
0x050F	7:0	R/W	FAST_BW1_PLLB	
0x0510	7:0	R/W	FAST_BW2_PLLB	
0x0511	7:0	R/W	FAST_BW3_PLLB	
0x0512	7:0	R/W	FAST_BW4_PLLB	
0x0513	7:0	R/W	FAST_BW5_PLLB	

This group of registers determines the DSPLL Fastlock bandwidth. In ClockBuilder Pro, it is selectable from 10 Hz to 4 kHz in factors of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 13.167. Register 0x0514 DSPLL Bandwidth Update for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0514	0	S	BW_UPDATE_PLLB	Set to 1 to latch updated BWx_PLLB and FAST_BWx_PLLB bandwidth registers into operation.

Setting this self-clearing bit high latches all of the new DSPLL B bandwidth register values into operation. Asserting this strobe will update all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB bandwidths at the same time. A device Soft Reset (0x001C[0]) will have the same effect, but individual DSPLL soft resets will not update these values.

Table 13.168. Register 0x0515-0x051B M Feedback Divider Numerator, 56-bits for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0515	7:0	R/W	M_NUM_PLLB	M feedback divider Numerator 56-bit Integer
0x0516	15:8			
0x0517	23:16			
0x0518	31:24			
0x0519	39:32			
0x051A	47:40			
0x051B	55:48			

Note that DSPLL B includes a divide-by-5 block in the PLL feedback path before the M divider. Register values for the DSPLL B M divider must account for this additional divider. This divider is not present in DSPLLs A, C, or D.

Table 13.169. Register 0x051C-0x051F M Feedback Divider Denominator, 32-bits for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x051C	7:0	R/W	M_DEN_PLLB	M feedback divider Denominator 32-bit Integer
0x051D	15:8			
0x051E	23:16			
0x051F	31:24			

The DSPLL M feedback divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. An Integer ratio of (M_NUM / M_DEN) will give the best phase noise performance.

Note: There is a divide-by-5 prescaler before the DSPLL B M divider, so if (M_NUM / M_DEN) = 100, the effective feedback divide ratio (Fvco / Fpfd) will be 500.

Table 13.170. Register 0x0520 M Divider Update for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0520	0	S	M_UPDATE_PLLB	Set this bit to latch the M feedback divider register values into operation.

Setting this self-clearing bit high latches the new M feedback divider register values into operation. A Soft Reset will have the same effect.

Table 13.171. Register 0x0521 M Divider Fractional Enable for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0521	3:0	R/W	M_FRAC_MODE_PLLB	M feedback divider fractional mode. Must be set to 0xB for proper operation
0x0521	4	R/W	M_FRAC_EN_PLLB	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0521	5	R/W	Reserved	Must be set to 1

Table 13.172. Register 0x052A Input Clock Select for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x052A	0	R/W	IN_SEL_REGCTRL_PLLB	Manual Input Select control source. 0: Pin controlled input clock selection (default) 1: IN_SEL register input clock selection (ZDM_IN_SEL in ZDM)
0x052A	3:1	R/W	IN_SEL_PLLB	Manual Input Select selection register. (Non-ZDM) 0: IN0 (default), 1: IN1, 2: IN2, 3: IN3, 4-7: Reserved

Input clock selection for manual register based and pin controlled clock selection. Note that in ZDM, the ZDM_IN_SEL (0x0487[2:1]) input source select control bits are used and IN_SEL is ignored. In both ZDM and non-ZDM operation, IN_SEL_REGCTRL determines whether register-based or pin-based manual source selection is used.

Note: When IN_SEL_REGCTRL is low, IN_SEL does not do anything and the clock selection is pin controlled.

Table 13.173. Register 0x052B Fastlock Control for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN_PLLB	Auto Fastlock Enable/Disable. 0: Disable Auto Fastlock (default) 1: Enable Auto Fastlock
0x052B	1	R/W	FASTLOCK_MAN_PLLB	Manually Force Fastlock. 0: Normal Operation (default) 1: Force Fastlock

When Fastlock is enabled by either manual or automatic means, the higher Fastlock bandwidth will be used to provide faster settling of the DSPLL. With FASTLOCK_MAN_PLLB=0 and FASTLOCK_AUTO_EN_PLLB=1, the DSPLL will automatically revert to the loop bandwidth when the loop has locked and LOL deasserts. See 1.4.1 Fastlock for more information on Fastlock behavior.

Table 13.174. Register 0x052C Holdover Exit Control for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x052C	0	R/W	HOLD_EN_PLLB	Holdover enable 0: Holdover Disabled 1: Holdover Enabled (default)
0x052C	3	R/W	HOLD_RAMP_BYP_PLLB	Must be set to 1 for Normal Operation.
0x052C	4	R/W	HOLD_EXIT_BW_SEL_PLLB	Selects the exit from Holdover bandwidth when ramped exit is disabled by the user. 0: Exit Holdover using Fastlock bandwidth (default) 1: Exit Holdover using the DSPLL loop bandwidth
0x052C	7:5	R/W	HOLD_RAMP_RATE_PLLB	Sets the base rate for ramped input switching and Holdover Entry/Exit. This value is multiplied by the RAMP_STEP_ADJ_PLLB factor to find the ramp rate. 0: 1.48ppm/s 1: 2.22ppm/s 2: 2.53ppm/s 3: 1.18ppm/s 4: 0.74 ppm/s 5: 5.06 ppm/s 6: 10.12 ppm/s 7: 40.48 ppm/s Ramp Rate = HOLD_RAMP_RATE_PLLB * RAMP_STEP_ADJ_PLLB

When a valid input is presented to the DSPLL while the device is in Holdover or Freerun mode, the higher Fastlock bandwidth can be enabled to provide faster DSPLL settling. When a slower response is desired, then the regular loop bandwidth may be used instead.

Table 13.175. Register 0x052E Holdover History Average Length for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN_PLLB	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds: Window Length = $(2^{HOLD\_HIST\_LEN\_PLLB} - 1) \times 8 / 3 \times 10^{-7}$

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See 2.5 Holdover Mode to calculate the window length from the register value.

Table 13.176. Register 0x052F Holdover History Delay for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x052F	4:0	R/W	HOLD_HIST_DELAY_PLLB	Delay Time to ignore data at the end of the historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $2^{HOLD\_HIST\_DELAY\_PLLB} \times 2 / 3 \times 10^{-7}$

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See 2.5 Holdover Mode to calculate the ignore delay time from the register value.

Table 13.177. Register 0x0532-0x0524 Holdover Cycle Count DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0532	7:0	R/W	HOLD_15M_CYC_COUNT_PLLB	Value calculated in CBPro.
0x0533	15:8	R/W	HOLD_15M_CYC_COUNT_PLLB	
0x0534	23:16	R/W	HOLD_15M_CYC_COUNT_PLLB	

Table 13.178. Register 0x0535 Force Holdover for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0535	0	R/W	FORCE_HOLD_PLLB	Force the device into Holdover mode. Used to hold the device output clocks while retraining an upstream input clock. 0: Normal Operation 1: Force Holdover/Freerun Mode: HOLD_HIST_VALID_PLLB = 0 => Freerun Mode HOLD_HIST_VALID_PLLB = 1 => Holdover Mode

Table 13.179. Register 0x0536 Input Clock Switching Control for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0536	1:0	R/W	CLK_SWITCH_MODE_PLLB	Selects manual or automatic switching modes. Automatic mode can be Revertive or Non-revertive. 0: Manual (default) 1: Automatic Non-revertive 2: Automatic Revertive 3: Reserved

Reg Address	Bit Field	Type	Name	Description
0x0536	2	R/W	HSW_EN_PLLB	Enable Hitless Switching. 0: Disable Hitless switching (default) 1: Enable Hitless switching (phase buildout enabled)

Table 13.180. Register 0x0537 Input Fault Masks for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0537	3:0	R/W	IN_LOS_MSK_PLLB	Enables the use of IN3 - IN0 LOS status in determining a valid clock for automatic input selection. 0: Use LOS in automatic clock switching logic (default) 1: Mask (ignore) LOS from automatic clock switching logic
0x0537	7:4	R/W	IN_OOF_MSK_PLLB	Determines the OOF status for IN3 - IN0 and is used in determining a valid clock for the automatic input selection. 0: Use OOF in the automatic clock switching logic (default) 1: Mask (ignore) OOF from automatic clock switching logic

This register is for the input clock fault masks. For each of the four clock inputs, the OOF and/or the LOS fault can be used for the clock selection logic or they can be masked from it.

Note: The clock selection logic can affect entry into Holdover.

Table 13.181. Register 0x0538-0x0539 Clock Input Priorities for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0538	2:0	R/W	IN0_PRIORITY_PLLB	IN0 - IN3 priority assignment for the automatic switching state machine. Priority assignments in descending importance are: 1, 2, 3, 4 (or 0 for no priority) 5-7: Reserved
0x0538	6:4	R/W	IN1_PRIORITY_PLLB	
0x0539	2:0	R/W	IN2_PRIORITY_PLLB	
0x0539	6:4	R/W	IN3_PRIORITY_PLLB	

This register is used to assign priority to each input clock for automatic clock input switching. The available clock with the highest priority will be selected. Priority 1 is first and most likely to be selected, followed by priorities 2-4. Priority 0 prevents the clock input from being automatically selected, though it may still be manually selected. When two valid input clocks are assigned the same priority, the lowest numbered input will be selected. In other words, IN0 has priority over IN1-IN3, IN1 has priority over IN2-IN3, etc, when the priorities are the same.

Table 13.182. Register 0x053A Hitless Switching Mode DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x053A	1:0	R/W	HSW_MODE_PLLB	1: Default setting, do not modify 0, 2, 3: Reserved
0x053A	3:2	R/W	HSW_PHMEAS_CTRL_PLLB	0: Default setting, do not modify 1, 2, 3: Reserved

Table 13.183. Register 0x053B–0x053C Hitless Switching Phase Threshold DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x053B	7:0	R/W	HSW_PHMEAS_THR_PLLB	Value calculated in CBPro.
0x053C	9:8	R/W	HSW_PHMEAS_THR_PLLB	

Table 13.184. Register 0x053D Hitless Switching Length DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x053D	4:0	R/W	HSW_COARSE_PM_LEN_PLLB	Value calculated in CBPro.

Table 13.185. Register 0x053E Hitless Switching Length DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x053E	4:0	R/W	HSW_COARSE_PM_DLY_PLLB	Value calculated in CBPro.

Table 13.186. Register 0x053F DSPLL Hold Valid and Fastlock Status for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x053F	1	R	HOLD_HIST_VALID_PLLB	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x053F	2	R	FASTLOCK_STATUS_PLLB	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLB accumulation will stop. When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 13.187. Register 0x0540 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0540	7:0	R/W	RESERVED	Reserved.

This register is used when making certain changes to the device. See Section 2.1.1 Updating Registers During Device Operation for more information.

Table 13.188. Register 0x0588 Fine Hitless Switching PM Length for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0588	3:0	R/W	HSW_FINE_PM_LEN_PLLB	Values set by CBPro.

Table 13.189. Register 0x0589 - 0x059A PFD Enable Delay for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0589	7:0	R/W	PFD_EN_DELAY_PLLB	Set by CBPro.
0x058A	12:8	R/W	PFD_EN_DELAY_PLLB	

Table 13.190. Register 0x059B Holdover Exit for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x059B	1	R/W	INIT_LP_CLOSE_HO_PLLB	PLL acquisition method for Freerun to Lock transition. 0: Normal loop closure 1: Holdover exit ramp (default)
0x059B	4	R/W	HOLD_PRESERVE_HIST_PLLB	Preserve Holdover history when the input clock is lost or switched. 0: Clear Holdover history when the input clock is lost or switched. 1: Preserve Holdover history when the input clock is lost or switched. (default)
0x059B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLB	Holdover Freeze control when the input clock is lost or switched. 0: Use filter output on Freeze. 1: Use Integrator-only on Freeze. (default)
0x059B	6	R/W	HOLDEXIT_BW_SEL0_PLLB	Set by CBPro.
0x059B	7	R/W	HOLDEXIT_STD_BO_PLLB	1: Default setting, do not modify 0: Reserved

Table 13.191. Register 0x059C Holdover Exit Control for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x059C	6	R/W	HOLDEX-IT_ST_BO_PLLB	Value set by CBPro.
0x059C	7	R/W	HOLD_RAMPBP_NO HIST_PLLB	Value set by CBPro.

Table 13.192. Register 0x059D-0x05A2 Holdover Exit Bandwidth for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x059D	7:0	R/W	HOLDEX-IT_BW0_PLLB	DSPLL B Holdover Exit bandwidth parameters calculated by CBPro when ramp switching is disabled.
0x059E	7:0	R/W	HOLDEX-IT_BW1_PLLB	
0x059F	7:0	R/W	HOLDEX-IT_BW2_PLLB	
0x05A0	7:0	R/W	HOLDEX-IT_BW3_PLLB	
0x05A1	7:0	R/W	HOLDEX-IT_BW4_PLLB	
0x05A2	7:0	R/W	HOLDEX-IT_BW5_PLLB	

This group of registers determines the DSPLL B bandwidth used when exiting Holdover Mode. In ClockBuilder Pro it is selectable from 10 Hz to 100 Hz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that the individual SOFT_RST_PLLB (0x001C[2]) does not update these bandwidth parameters.

Table 13.193. Register 0x05A4 Hitless Switching Limit for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05A4	7:0	R/W	HSW_LIMIT_PLLB	Value set by CBPro.

Table 13.194. Register 0x05A5 Hitless Switching Limit Action for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05A5	0	R/W	HSW_LIMIT_AC-TION_PLLB	Value set by CBPro.

Table 13.195. Register 0x05A6 Hitless Switching Ramp Control for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05A6	2:0	R/W	RAMP_STEP_ADJ_PLLB	Scaling factor for ramped input switching and Holdover Entry/Exit. Multiply with HOLD_RAMP_RATE_PLLB to calculate final ramp rate. 0: 1x 1: 4x 2: 16x 3: 64x 4: 256x 5: 1024x 6: 1/4x 7: 1/2x Ramp Rate = HOLD_RAMP_RATE_PLLB * RAMP_STEP_ADJ_PLLB
0x05A6	3	R/W	RAMP_SWITCH_EN_PLLB	Enable ramped input switching and entry into Holdover/Freerun. 0: Disable ramped input switching and entry into Holdover 1: Enable ramped input switching and entry into Holdover

Table 13.196. Register 0x05AC Configuration for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05AC	0	R/W	OUT_MAX_LIMIT_EN_PLLB	Set by CBPro.
0x05AC	3	R/W	HOLD_SETTLE_DET_EN_PLLB	Set by CBPro.

Table 13.197. Register 0x05AD - 0x05AE Configuration for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05AD	7:0	R/W	OUT_MAX_LIMIT_LMT_PLLB	Set by CBPro.
0x05AE	15:0	R/W		

Table 13.198. Register 0x05B1 - 0x05B2 Configuration for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05B1	7:0	R/W	HOLD_SETTLE_TARGET_PLLB	Set by CBPro.
0x05B2	15:0	R/W		

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Table 13.199. Register 0x0607 Input Selection for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0607	7:6	R	IN_ACTV_PLLC	Currently selected DSPLL C input clock. 0: IN0 1: IN1 2: IN2 3: IN3

This register displays the currently selected input for the DSPLL. In manual select mode, this reflects either the register value or the voltages on the IN_SEL1 and IN_SEL0 pins. In automatic switching mode, it reflects the input currently chosen by the automatic algorithm. If there are no valid input clocks in the automatic mode, this value will retain its previous value until a valid input clock is presented. Note that this value is not meaningful in Holdover or Freerun modes.

Table 13.200. Register 0x0608-0x060D DSPLL Loop Bandwidth for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0608	7:0	R/W	BW0_PLLC	DSPLL C loop bandwidth parameters.
0x0609	7:0	R/W	BW1_PLLC	
0x060A	7:0	R/W	BW2_PLLC	
0x060B	7:0	R/W	BW3_PLLC	
0x060C	7:0	R/W	BW4_PLLC	
0x060D	7:0	R/W	BW5_PLLC	

This group of registers determines the DSPLL C loop bandwidth. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLC bit (reg 0x0614[0]) must be used to cause all of the BWx_PLLC, FAST_BWx_PLLC, and BWx_HO_PLLC parameters to take effect. Note that individual SOFT_RST_PLLC (0x001C[3]) does not update the bandwidth parameters.

Table 13.201. Register 0x060E-0x0613 DSPLL Fastlock Loop Bandwidth for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x060E	7:0	R/W	FAST_BW0_PLLC	DSPLL C Fastlock Bandwidth parameters.
0x060F	7:0	R/W	FAST_BW1_PLLC	
0x0610	7:0	R/W	FAST_BW2_PLLC	
0x0611	7:0	R/W	FAST_BW3_PLLC	
0x0612	7:0	R/W	FAST_BW4_PLLC	
0x0613	7:0	R/W	FAST_BW5_PLLC	

This group of registers determines the DSPLL Fastlock bandwidth. In ClockBuilder Pro, it is selectable from 200 Hz to 4 kHz in factors of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLC bit (reg 0x0614[0]) must be used to cause all of the BWx_PLLC, FAST_BWx_PLLC, and BWx_HO_PLLC parameters to take effect. Note that individual SOFT_RST_PLLC (0x001C[3]) does not update the bandwidth parameters.

Table 13.202. Register 0x0614 DSPLL Bandwidth Update for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0614	0	S	BW_UPDATE_PLLC	Set to 1 to latch updated BWx_PLLC and FAST_BWx_PLLC bandwidth registers into operation.

Setting this self-clearing bit high latches all of the new DSPLL C bandwidth register values into operation. Asserting this strobe will update all of the BWx_PLLC, FAST_BWx_PLLC, and BWx_HO_PLLC bandwidths at the same time. A device Soft Reset (0x001C[0]) will have the same effect, but individual DSPLL soft resets will not update these values.

Table 13.203. Register 0x0615-0x061B M Feedback Divider Numerator, 56-bits for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0615	7:0	R/W	M_NUM_PLLC	M feedback divider Numerator 56-bit Integer
0x0616	15:8			
0x0617	23:16			
0x0618	31:24			
0x0619	39:32			
0x061A	47:40			
0x061B	55:48			

Table 13.204. Register 0x061C-0x061F M Feedback Divider Denominator, 32-bits for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x061C	7:0	R/W	M_DEN_PLLC	M feedback divider Denominator 32-bit Integer
0x061D	15:8			
0x061E	23:16			
0x061F	31:24			

The DSPLL M feedback divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. An Integer ratio of (M_NUM / M_DEN) will give the best phase noise performance.

Table 13.205. Register 0x0620 M Divider Update for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0620	0	S	M_UPDATE_PLLC	Set this bit to latch the M feedback divider register values into operation.

Setting this self-clearing bit high latches the new M feedback divider register values into operation. A Soft Reset will have the same effect.

Table 13.206. Register 0x0621 M Divider Fractional Enable for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0621	3:0	R/W	M_FRAC_MODE_PLLC	M feedback divider fractional mode. Must be set to 0xB for proper operation

Reg Address	Bit Field	Type	Name	Description
0x0621	4	R/W	M_FRAC_EN_PLLC	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0621	5	R/W	Reserved	Must be set to 1 for DSPLL C

Table 13.207. Register 0x0622 M Divider DSO Step Mask for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0622	0	R/W	M_FSTEPW_MASK_PLLC	M feedback divider DCO mask 0: Enable FINC/FDEC Updates (default) 1: Disable FINC/FDEC Updates

Table 13.208. Register 0x0623-0x0629 M Divider DCO FSTEPW for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0623	7:0	R/W	M_FSTEPW_PLLC	56-bit number
0x0624	15:8			
0x0625	23:16			
0x0626	31:24			
0x0627	39:32			
0x0628	47:40			
0x0629	55:48			

Table 13.209. Register 0x062A Input Clock Select for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x062A	2:0	R/W	IN_SEL_PLLC	Manual Input Select selection register. 0: IN0 (default), 1: IN1, 2: IN2, 3: IN3 4-7: Reserved

Input clock selection for manual register based and pin controlled clock selection.

Note: When IN_SEL_REGCTRL is low, IN_SEL does not do anything and the clock selection is pin controlled.

Table 13.210. Register 0x062B Fastlock Control for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x062B	0	R/W	FASTLOCK_AUTO_EN_PLLC	Auto Fastlock Enable/Disable. 0: Disable Auto Fastlock (default) 1: Enable Auto Fastlock

Reg Address	Bit Field	Type	Name	Description
0x062B	1	R/W	FASTLOCK_MAN_PLLC	Manually Force Fastlock. 0: Normal Operation (default) 1: Force Fastlock

When Fastlock is enabled by either manual or automatic means, the higher Fastlock bandwidth will be used to provide faster settling of the DSPLL. With FASTLOCK_MAN_PLLC=0 and FASTLOCK_AUTO_EN_PLLC=1, the DSPLL will automatically revert to the loop bandwidth when the loop has locked and LOL deasserts. See 1.4.1 Fastlock for more information on Fastlock behavior.

Table 13.211. Register 0x062C Holdover Exit Control for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x062C	0	R/W	HOLD_EN_PLLC	Holdover enable 0: Holdover Disabled 1: Holdover Enabled (default)
0x062C	3	R/W	HOLD_RAMP_BYP_PLLC	Must be set to 1 for Normal Operation.
0x062C	4	R/W	HOLD_EXIT_BW_SEL_PLLC	Selects the exit rate from Holdover bandwidth. 0: Exit Holdover using Fastlock bandwidth (default) 1: Exit Holdover using the DSPLL loop bandwidth
0x062C	7:5	R/W	HOLD_RAMP_RATE_PLLC	Sets the base rate for ramped input switching and Holdover Entry/Exit. This value is multiplied by the RAMP_STEP_ADJ_PLLC factor to find the ramp rate. 0: 1.48 ppm/s 1: 2.22 ppm/s 2: 2.53 ppm/s 3: 1.18 ppm/s 4: 0.74 ppm/s 5: 5.06 ppm/s 6: 10.12 ppm/s 7: 40.48 ppm/s Ramp Rate = HOLD_RAMP_RATE_PLLC * RAMP_STEP_ADJ_PLLC

When a valid input is presented to the DSPLL while the device is in Holdover or Freerun mode, the higher Fastlock bandwidth can be enabled to provide faster DSPLL settling. When a slower response is desired, then the regular loop bandwidth may be used instead.

Table 13.212. Register 0x062E Holdover History Average Length for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x062E	4:0	R/W	HOLD_HIST_LEN_PLLC	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds: Window Length = $(2^{HOLD\_HIST\_LEN\_PLLC} - 1) \times 8 / 3 \times 10^{-7}$

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See 2.5 Holdover Mode to calculate the window length from the register value.

Table 13.213. Register 0x062F Holdover History Delay for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x062F	4:0	R/W	HOLD_HIST_DELAY_PLLC	Delay Time to ignore data at the end of the historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $2^{HOLD\_HIST\_DELAY\_PLLC} \times 2 / 3 \times 10^{-7}$

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See 2.5 Holdover Mode to calculate the ignore delay time from the register value.

Table 13.214. Register 0x0632-0x0634 Holdover Cycle Count DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0632	7:0	R/W	HOLD_15M_CYC_COUNT_PLLC	Value calculated in CBPro.
0x0633	15:8	R/W	HOLD_15M_CYC_COUNT_PLLC	
0x0634	23:16	R/W	HOLD_15M_CYC_COUNT_PLLC	

Table 13.215. Register 0x0635 Force Holdover for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0635	0	R/W	FORCE_HOLD_PLLC	Force the device into Holdover mode. Used to hold the device output clocks while retraining an upstream input clock. 0: Normal Operation 1: Force Holdover/Freerun Mode: HOLD_HIST_VALID_PLLC = 0 => Freerun Mode HOLD_HIST_VALID_PLLC = 1 => Holdover Mode

Table 13.216. Register 0x0636 Input Clock Switching Control for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0636	1:0	R/W	CLK_SWITCH_MODE_PLLC	Selects manual or automatic switching modes. Automatic mode can be Revertive or Non-revertive. 0: Manual (default) 1: Automatic Non-revertive 2: Automatic Revertive 3: Reserved
0x0636	2	R/W	HSW_EN_PLLC	Enable Hitless Switching. 0: Disable Hitless switching (default) 1: Enable Hitless switching (phase buildout enabled)

Table 13.217. Register 0x0637 Input Fault Masks for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0637	3:0	R/W	IN_LOS_MSK_PLLC	Enables the use of IN3 - IN0 LOS status in determining a valid clock for automatic input selection. 0: Use LOS in automatic clock switching logic (default) 1: Mask (ignore) LOS from automatic clock switching logic

Reg Address	Bit Field	Type	Name	Description
0x0637	7:4	R/W	IN_OOF_MSK_PLLC	Determines the OOF status for IN3 - IN0 and is used in determining a valid clock for the automatic input selection. 0: Use OOF in the automatic clock switching logic (default) 1: Mask (ignore) OOF from automatic clock switching logic

This register is for the input clock fault masks. For each of the four clock inputs, the OOF and/or the LOS fault can be used for the clock selection logic or they can be masked from it.

Note: The clock selection logic can affect entry into Holdover.

Table 13.218. Register 0x0638-0x0639 Clock Input Priorities for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0638	2:0	R/W	IN0_PRIORITY_PLLC	IN0 - IN3 priority assignment for the automatic switching state machine. Priority assignments in descending importance are: 1, 2, 3, 4 (or 0 for never select) 5-7: Reserved
0x0638	6:4	R/W	IN1_PRIORITY_PLLC	
0x0639	2:0	R/W	IN2_PRIORITY_PLLC	
0x0639	6:4	R/W	IN3_PRIORITY_PLLC	

This register is used to assign priority to each input clock for automatic clock input switching. The available clock with the highest priority will be selected. Priority 1 is first and most likely to be selected, followed by priorities 2-4. Priority 0 prevents the clock input from being automatically selected, though it may still be manually selected. When two valid input clocks are assigned the same priority, the lowest numbered input will be selected. In other words, IN0 has priority over IN1-IN3, IN1 has priority over IN2-IN3, etc, when the priorities are the same.

Table 13.219. Register 0x063A Hitless Switching Mode DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x063A	1:0	R/W	HSW_MODE_PLLC	1: Default setting, do not modify 0, 2, 3: Reserved
0x063A	3:2	R/W	HSW_PHMEAS_CTRL_PLLC	0: Default setting, do not modify 1, 2, 3: Reserved

Table 13.220. Register 0x063B–0x063C Hitless Switching Phase Threshold DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x063B	7:0	R/W	HSW_PHMEAS_THR_PLLC	Value calculated in CBPro.
0x063C	9:8	R/W	HSW_PHMEAS_THR_PLLC	

Table 13.221. Register 0x063D Hitless Switching Length DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x063D	4:0	R/W	HSW_COARSE_PM_LEN_PLLC	Value calculated in CBPro.

Table 13.222. Register 0x063E Hitless Switching Length DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x063E	4:0	R/W	HSW_COARSE_PM_DLY_PLLC	Value calculated in CBPro.

Table 13.223. Register 0x063F DSPLL Hold Valid and Fastlock Status for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x063F	1	R	HOLD_HIST_VALID_PLLC	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x063F	2	R	FASTLOCK_STATUS_PLLC	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLC accumulation will stop. When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 13.224. Register 0x0688 Fine Hitless Switching PM Length for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0688	3:0	R/W	HSW_FINE_PM_LEN_PLLC	Values set by CBPro.

Table 13.225. Register 0x0689 - 0x069A PFD Enable Delay for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x0689	7:0	R/W	PFD_EN_DELAY_PLLC	Set by CBPro.
0x068A	12:8	R/W	PFD_EN_DELAY_PLLC	

Table 13.226. Register 0x069B Holdover Exit for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x069B	1	R/W	INIT_LP_CLOSE_HO_PLLC	PLL acquisition method for Freerun to Lock transition. 0: Normal loop closure 1: Holdover exit ramp (default)

Reg Address	Bit Field	Type	Name	Description
0x069B	4	R/W	HOLD_PRE-SERVE_HIST_PLLC	Preserve Holdover history when the input clock is lost or switched. 0: Clear Holdover history when the input clock is lost or switched. 1: Preserve Holdover history when the input clock is lost or switched. (default)
0x069B	5	R/W	HOLD_FRZ_WITH_IN TONLY_PLLC	Holdover Freeze control when the input clock is lost or switched. 0: Use filter output on Freeze. 1: Use Integrator-only on Freeze. (default)
0x069B	6	R/W	HOLDEX-IT_BW_SEL0_PLLC	Set by CBPro.
0x069B	7	R/W	HOLDEX-IT_STD_BO_PLLC	1: Default setting, do not modify 0: Reserved

Table 13.227. Register 0x069C Holdover Exit Control for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x069C	6	R/W	HOLDEX-IT_ST_BO_PLLC	Value set by CBPro.
0x069C	7	R/W	HOLD_RAMPBP_NO HIST_PLLC	Value set by CBPro.

Table 13.228. Register 0x069D-0x06A2 Holdover Exit Bandwidth for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x069D	7:0	R/W	HOLDEX-IT_BW0_PLLC	DSPLL C Holdover Exit bandwidth parameters calculated by CBPro when ramp switching is disabled.
0x069E	7:0	R/W	HOLDEX-IT_BW1_PLLC	
0x069F	7:0	R/W	HOLDEX-IT_BW2_PLLC	
0x06A0	7:0	R/W	HOLDEX-IT_BW3_PLLC	
0x06A1	7:0	R/W	HOLDEX-IT_BW4_PLLC	
0x06A2	7:0	R/W	HOLDEX-IT_BW5_PLLC	

This group of registers determines the DSPLL C bandwidth used when exiting Holdover Mode. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLC bit (reg 0x0614[0]) must be used to cause all of the BWx_PLLC, FAST_BWx_PLLC, and BWx_HO_PLLC parameters to take effect. Note that the individual SOFT_RST_PLLC (0x001C[3]) does not update these bandwidth parameters.

Table 13.229. Register 0x06A4 Hitless Switching Limit for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x06A4	7:0	R/W	HSW_LIMIT_PLLC	Value set by CBPro.

Table 13.230. Register 0x06A5 Hitless Switching Limit Action for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x06A5	0	R/W	HSW_LIMIT_AC-TION_PLLC	Value set by CBPro.

Table 13.231. Register 0x06A6 Hitless Switching Ramp Control for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x06A6	2:0	R/W	RAMP_STEP_ADJ_PLLC	Scaling factor for ramped input switching and Holdover Entry/Exit. Multiply with HOLD_RAMP_RATE_PLLC to calculate final ramp rate. 0: 1x 1: 4x 2: 16x 3: 64x 4: 256x 5: 1024x 6: 1/4x 7: 1/2x Ramp Rate = HOLD_RAMP_RATE_PLLC * RAMP_STEP_ADJ_PLLC
0x06A6	3	R/W	RAMP_SWITCH_EN_PLLC	Enable ramped input switching and entry into Holdover/Freerun. 0: Disable ramped input switching and entry into Holdover 1: Enable ramped input switching and entry into Holdover

Table 13.232. Register 0x06AC Configuration for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x06AC	0	R/W	OUT_MAX_LIM-IT_EN_PLLC	Set by CBPro.
0x06AC	3	R/W	HOLD_SET-TLE_DET_EN_PLLC	Set by CBPro.

Table 13.233. Register 0x06AD - 0x06AE Configuration for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x06AD	7:0	R/W	OUT_MAX_LIM-IT_LMT_PLLC	Set by CBPro.
0x06AE	15:0	R/W		

Table 13.234. Register 0x6B1 - 0x06B2 Configuration for DSPLL C

Reg Address	Bit Field	Type	Name	Description
0x06B1	7:0	R/W	HOLD_SETTLE_TAR-GET_PLLC	Set by CBPro.
0x06B2	15:0	R/W		

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Table 13.235. Register 0x0708 Input Selection for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0708	7:6	R	IN_ACTV_PLLD	Currently selected DSPLL D input clock. 0: IN0 1: IN1 2: IN2 3: IN3

This register displays the currently selected input for the DSPLL. In manual select mode, this reflects either the register value or the voltages on the IN_SEL1 and IN_SEL0 pins. In automatic switching mode, it reflects the input currently chosen by the automatic algorithm. If there are no valid input clocks in the automatic mode, this value will retain its previous value until a valid input clock is presented. Note that this value is not meaningful in Holdover or Freerun modes.

Table 13.236. Register 0x0709-0x070E DSPLL Loop Bandwidth for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0709	7:0	R/W	BW0_PLLD	DSPLL D loop bandwidth parameters.
0x070A	7:0	R/W	BW1_PLLD	
0x070B	7:0	R/W	BW2_PLLD	
0x070C	7:0	R/W	BW3_PLLD	
0x070D	7:0	R/W	BW4_PLLD	
0x070E	7:0	R/W	BW5_PLLD	

This group of registers determines the DSPLL D loop bandwidth. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLD bit (reg 0x0715[0]) must be used to cause all of the BWx_PLLD, FAST_BWx_PLLD, and BWx_HO_PLLD parameters to take effect. Note that individual SOFT_RST_PLLD (0x001C[4]) does not update the bandwidth parameters.

Table 13.237. Register 0x070F-0x0714 DSPLL Fastlock Loop Bandwidth for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x070F	7:0	R/W	FAST_BW0_PLLD	DSPLL D Fastlock Bandwidth parameters.
0x0710	7:0	R/W	FAST_BW1_PLLD	
0x0711	7:0	R/W	FAST_BW2_PLLD	
0x0712	7:0	R/W	FAST_BW3_PLLD	
0x0713	7:0	R/W	FAST_BW4_PLLD	
0x0714	7:0	R/W	FAST_BW5_PLLD	

This group of registers determines the DSPLL Fastlock bandwidth. In ClockBuilder Pro, it is selectable from 200 Hz to 4 kHz in factors of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLD bit (reg 0x0715[0]) must be used to cause all of the BWx_PLLD, FAST_BWx_PLLD, and BWx_HO_PLLD parameters to take effect. Note that individual SOFT_RST_PLLD (0x001C[4]) does not update the bandwidth parameters.

Table 13.238. Register 0x0715 DSPLL Bandwidth Update for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0715	0	S	BW_UPDATE_PLLD	Set to 1 to latch updated BWx_PLLD and FAST_BWx_PLLD bandwidth registers into operation.

Setting this self-clearing bit high latches all of the new DSPLL D bandwidth register values into operation. Asserting this strobe will update all of the BWx_PLLD, FAST_BWx_PLLD, and BWx_HO_PLLD bandwidths at the same time. A device Soft Reset (0x001C[0]) will have the same effect, but individual DSPLL soft resets will not update these values.

Table 13.239. Register 0x0716-0x071C M Feedback Divider Numerator, 56-bits for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0716	7:0	R/W	M_NUM_PLLD	M feedback divider Numerator 56-bit Integer
0x0717	15:8			
0x0718	23:16			
0x0719	31:24			
0x071A	39:32			
0x071B	47:40			
0x071C	55:48			

Table 13.240. Register 0x071D-0x0720 M Feedback Divider Denominator, 32-bits for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x071D	7:0	R/W	M_DEN_PLLD	M feedback divider Denominator 32-bit Integer
0x071E	15:8			
0x071F	23:16			
0x0720	31:24			

The DSPLL M feedback divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. An Integer ratio of (M_NUM / M_DEN) will give the best phase noise performance.

Table 13.241. Register 0x0721 M Divider Update for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0721	0	S	M_UPDATE_PLLD	Set this bit to latch the M feedback divider register values into operation.

Setting this self-clearing bit high latches the new M feedback divider register values into operation. A Soft Reset will have the same effect.

Table 13.242. Register 0x0722 M Divider Fractional Enable for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0722	3:0	R/W	M_FRAC_MODE_PLLD	M feedback divider fractional mode. Must be set to 0xB for proper operation

Reg Address	Bit Field	Type	Name	Description
0x0722	4	R/W	M_FRAC_EN_PLLD	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0722	5	R/W	Reserved	Must be set to 1 for DSPLL D

Table 13.243. Register 0x0723 M Divider DSO Step Mask for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0723	0	R/W	M_FSTEPW_MASK_PLLD	M feedback divider DCO mask 0: Enable FINC/FDEC Updates (default) 1: Disable FINC/FDEC Updates

Table 13.244. Register 0x0724-0x072A M Divider DCO FSTEPW for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0724	7:0	R/W	M_FSTEPW_PLLD	56-bit number
0x0725	15:8			
0x0726	23:16			
0x0727	31:24			
0x0728	39:32			
0x0729	47:40			
0x072A	55:48			

Table 13.245. Register 0x072B Input Clock Select for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x072B	2:0	R/W	IN_SEL_PLLD	Manual Input Select selection register. 0: IN0 (default), 1: IN1, 2: IN2, 3: IN3 4-7: Reserved

Input clock selection for manual register based and pin controlled clock selection.

Note: When IN_SEL_REGCTRL is low, IN_SEL does not do anything and the clock selection is pin controlled.

Table 13.246. Register 0x072C Fastlock Control for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x072C	0	R/W	FASTLOCK_AUTO_EN_PLLD	Auto Fastlock Enable/Disable. 0: Disable Auto Fastlock (default) 1: Enable Auto Fastlock

Reg Address	Bit Field	Type	Name	Description
0x072C	1	R/W	FASTLOCK_MAN_PLLD	Manually Force Fastlock. 0: Normal Operation (default) 1: Force Fastlock

When Fastlock is enabled by either manual or automatic means, the higher Fastlock bandwidth will be used to provide faster settling of the DSPLL. With FASTLOCK_MAN_PLLD=0 and FASTLOCK_AUTO_EN_PLLD=1, the DSPLL will automatically revert to the loop bandwidth when the loop has locked and LOL deasserts. See 1.4.1 Fastlock for more information on Fastlock behavior.

Table 13.247. Register 0x072D Holdover Exit Control for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x072D	0	R/W	HOLD_EN_PLLD	Holdover enable 0: Holdover Disabled 1: Holdover Enabled (default)
0x072D	3	R/W	HOLD_RAMP_BYP_PLLD	Must be set to 1 for Normal Operation.
0x072D	4	R/W	HOLD_EXIT_BW_SEL_PLLD	Selects the exit rate from Holdover bandwidth. 0: Exit Holdover using Fastlock bandwidth (default) 1: Exit Holdover using the DSPLL loop bandwidth
0x072D	7:5	R/W	HOLD_RAMP_RATE_PLLD	Sets the base rate for ramped input switching and Holdover Entry/Exit. This value is multiplied by the RAMP_STEP_ADJ_PLLD factor to find the ramp rate. 0: 1.48 ppm/s 1: 2.22 ppm/s 2: 2.53 ppm/s 3: 1.18 ppm/s 4: 0.74 ppm/s 5: 5.06 ppm/s 6: 10.12 ppm/s 7: 40.48 ppm/s Ramp Rate = HOLD_RAMP_RATE_PLLD * RAMP_STEP_ADJ_PLLD

When a valid input is presented to the DSPLL while the device is in Holdover or Freerun mode, the higher Fastlock bandwidth can be enabled to provide faster DSPLL settling. When a slower response is desired, then the regular loop bandwidth may be used instead.

Table 13.248. Register 0x072F Holdover History Average Length for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x072F	4:0	R/W	HOLD_HIST_LEN_PLLD	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds: Window Length = $(2^{HOLD\_HIST\_LEN\_PLLD} - 1) \times 8 / 3 \times 10^{-7}$

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See 2.5 Holdover Mode to calculate the window length from the register value.

Table 13.249. Register 0x0730 Holdover History Delay for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0730	4:0	R/W	HOLD_HIST_DELAY_PLLD	Delay Time to ignore data at the end of the historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $2^{HOLD\_HIST\_DELAY\_PLLD} \times 2 / 3 \times 10^{-7}$

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See 2.5 Holdover Mode to calculate the ignore delay time from the register value.

Table 13.250. Register 0x0733-x0735 Holdover Cycle Count DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0733	7:0	R/W	HOLD_15M_CYC_COUNT_PLLD	Value calculated in CBPro.
0x0734	15:8	R/W	HOLD_15M_CYC_COUNT_PLLD	
0x0735	23:16	R/W	HOLD_15M_CYC_COUNT_PLLD	

Table 13.251. Register 0x0736 Force Holdover for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0736	0	R/W	FORCE_HOLD_PLLD	Force the device into Holdover mode. Used to hold the device output clocks while retraining an upstream input clock. 0: Normal Operation 1: Force Holdover/Freerun Mode: HOLD_HIST_VALID_PLLD = 0 => Freerun Mode HOLD_HIST_VALID_PLLD = 1 => Holdover Mode

Table 13.252. Register 0x0737 Input Clock Switching Control for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0737	1:0	R/W	CLK_SWITCH_MODE_PLLD	Selects manual or automatic switching modes. Automatic mode can be Revertive or Non-revertive. 0: Manual (default) 1: Automatic Non-revertive 2: Automatic Revertive 3: Reserved
0x0737	2	R/W	HSW_EN_PLLD	Enable Hitless Switching. 0: Disable Hitless switching (default) 1: Enable Hitless switching (phase buildout enabled)

Table 13.253. Register 0x0738 Input Fault Masks for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0738	3:0	R/W	IN_LOS_MSK_PLLD	Enables the use of IN3 - IN0 LOS status in determining a valid clock for automatic input selection. 0: Use LOS in automatic clock switching logic (default) 1: Mask (ignore) LOS from automatic clock switching logic

Reg Address	Bit Field	Type	Name	Description
0x0738	7:4	R/W	IN_OOF_MSK_PLLD	Determines the OOF status for IN3 - IN0 and is used in determining a valid clock for the automatic input selection. 0: Use OOF in the automatic clock switching logic (default) 1: Mask (ignore) OOF from automatic clock switching logic

This register is for the input clock fault masks. For each of the four clock inputs, the OOF and/or the LOS fault can be used for the clock selection logic or they can be masked from it.

Note: The clock selection logic can affect entry into Holdover.

Table 13.254. Register 0x0739-0x073A Clock Input Priorities for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0739	2:0	R/W	IN0_PRIORITY_PLLD	IN0 - IN3 priority assignment for the automatic switching state machine. Priority assignments in descending importance are: 1, 2, 3, 4 (or 0 for never select) 5-7: Reserved
0x0739	6:4	R/W	IN1_PRIORITY_PLLD	
0x073A	2:0	R/W	IN2_PRIORITY_PLLD	
0x073A	6:4	R/W	IN3_PRIORITY_PLLD	

This register is used to assign priority to each input clock for automatic clock input switching. The available clock with the highest priority will be selected. Priority 1 is first and most likely to be selected, followed by priorities 2-4. Priority 0 prevents the clock input from being automatically selected, though it may still be manually selected. When two valid input clocks are assigned the same priority, the lowest numbered input will be selected. In other words, IN0 has priority over IN1-IN3, IN1 has priority over IN2-IN3, etc, when the priorities are the same.

Table 13.255. Register 0x073B Hitless Switching Mode DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x073B	1:0	R/W	HSW_MODE_PLLD	1: Default setting, do not modify 0, 2, 3: Reserved
0x073B	3:2	R/W	HSW_PHMEAS_CTRL_PLLD	0: Default setting, do not modify 1, 2, 3: Reserved

Table 13.256. Register 0x073C–0x073D Hitless Switching Phase Threshold DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x073C	7:0	R/W	HSW_PHMEAS_THR_PLLD	Value calculated in CBPro.
0x073D	9:8	R/W	HSW_PHMEAS_THR_PLLD	

Table 13.257. Register 0x073E Hitless Switching Length DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x073E	4:0	R/W	HSW_COARSE_PM_LEN_PLLD	Value calculated in CBPro.

Table 13.258. Register 0x073F Hitless Switching Length DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x073F	4:0	R/W	HSW_COARSE_PM_DLY_PLLD	Value calculated in CBPro.

Table 13.259. Register 0x0740 DSPLL Hold Valid and Fastlock Status for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0740	1	R	HOLD_HIST_VALID_PLLD	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x0740	2	R	FASTLOCK_STATUS_PLLD	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLD accumulation will stop. When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 13.260. Register 0x0788 Fine Hitless Switching PM Length for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0788	3:0	R/W	HSW_FINE_PM_LEN_PLLD	Values set by CBPro.

Table 13.261. Register 0x0789-0x078A PFD Enable Delay for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x0789	7:0	R/W	PFD_EN_DELAY_PLLD	Set by CBPro.
0x078A	12:8	R/W	PFD_EN_DELAY_PLLD	

Table 13.262. Register 0x079B Holdover Exit for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x079B	1	R/W	INIT_LP_CLOSE_HO_PLLD	PLL acquisition method for Freerun to Lock transition. 0: Normal loop closure 1: Holdover exit ramp (default)

Reg Address	Bit Field	Type	Name	Description
0x079B	4	R/W	HOLD_PRE-SERVE_HIST_PLLD	Preserve Holdover history when the input clock is lost or switched. 0: Clear Holdover history when the input clock is lost or switched. 1: Preserve Holdover history when the input clock is lost or switched. (default)
0x079B	5	R/W	HOLD_FRZ_WITH_IN TONLY_PLLD	Holdover Freeze control when the input clock is lost or switched. 0: Use filter output on Freeze. 1: Use Integrator-only on Freeze. (default)
0x079B	6	R/W	HOLDEX-IT_BW_SEL0_PLLD	Set by CBPro.
0x079B	7	R/W	HOLDEX-IT_STD_BO_PLLD	1: Default setting, do not modify 0: Reserved

Table 13.263. Register 0x079C Holdover Exit Control for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x079C	6	R/W	HOLDEX-IT_ST_BO_PLLD	Value set by CBPro.
0x079C	7	R/W	HOLD_RAMPBP_NO HIST_PLLD	Value set by CBPro.

Table 13.264. Register 0x079D-0x07A2 Holdover Exit Bandwidth for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x079D	7:0	R/W	HOLDEX-IT_BW0_PLLD	DSPLL D Holdover Exit bandwidth parameters calculated by CBPro when ramp switching is disabled.
0x079E	7:0	R/W	HOLDEX-IT_BW1_PLLD	
0x079F	7:0	R/W	HOLDEX-IT_BW2_PLLD	
0x07A0	7:0	R/W	HOLDEX-IT_BW3_PLLD	
0x07A1	7:0	R/W	HOLDEX-IT_BW4_PLLD	
0x07A2	7:0	R/W	HOLDEXIT_ BW5_PLLD	

This group of registers determines the DSPLL D bandwidth used when exiting Holdover Mode. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLD bit (reg 0x0715[0]) must be used to cause all of the BWx_PLLD, FAST_BWx_PLLD, and BWx_HO_PLLD parameters to take effect. Note that the individual SOFT_RST_PLLD (0x001C[4]) does not update these bandwidth parameters.

Table 13.265. Register 0x07A4 Hitless Switching Limit for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x07A4	7:0	R/W	HSW_LIMIT_PLLD	Value set by CBPro.

Table 13.266. Register 0x07A5 Hitless Switching Limit Action for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x07A5	0	R/W	HSW_LIMIT_AC-TION_PLLD	Value set by CBPro.

Table 13.267. Register 0x07A6 Hitless Switching Ramp Control for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x07A6	2:0	R/W	RAMP_STEP_ADJ_PLLD	Scaling factor for ramped input switching and Holdover Entry/Exit. Multiply with HOLD_RAMP_RATE_PLLD to calculate final ramp rate. 0: 1x 1: 4x 2: 16x 3: 64x 4: 256x 5: 1024x 6: 1/4x 7: 1/2x Ramp Rate = HOLD_RAMP_RATE_PLLD * RAMP_STEP_ADJ_PLLD
0x07A6	3	R/W	RAMP_SWITCH_EN_PLLD	Enable ramped input switching and entry into Holdover/Freerun. 0: Disable ramped input switching and entry into Holdover 1: Enable ramped input switching and entry into Holdover

Table 13.268. Register 0x07AC Configuration for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x07AC	0	R/W	OUT_MAX_LIM-IT_EN_PLLD	Set by CBPro.
0x07AC	3	R/W	HOLD_SET-TLE_DET_EN_PLLD	Set by CBPro.

Table 13.269. Register 0x07AD - 0x07AE Configuration for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x07AD	7:0	R/W	OUT_MAX_LIM-IT_LMT_PLLD	Set by CBPro.
0x07AE	15:0	R/W		

Table 13.270. Register 0x07B1 - 0x07B2 Configuration for DSPLL D

Reg Address	Bit Field	Type	Name	Description
0x07B1	7:0	R/W	HOLD_SETTLE_TAR-GET_PLLD	Set by CBPro.
0x07B2	15:0	R/W		

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Table 13.271. Register 0x090E External XAXB Source Select

Reg Address	Bit Field	Type	Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	Must always be set to '1' for external XO operation on XA/XB.

Table 13.272. Register 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Name	Description
0x0943	0	R/W	IO_VDD_SEL	Select digital I/O operating voltage. 0: 1.8 V digital I/O connections 1: 3.3 V digital I/O connections

The IO_VDD_SEL configuration bit selects between 1.8V and 3.3V digital I/O. All digital I/O pins, including the serial interface pins, are 3.3V tolerant with either setting. The default 1.8V setting (0x0943 = 0x0) is the safe default choice that allows writes to the device regardless of the serial interface used or the host supply voltage. When the I^2C or SPI host is operating at 3.3V and the Si5381/82 at VDD=1.8V, the host must write IO_VDD_SEL=1 first. This will ensure that both the host and the serial interface are operating with the optimum signal thresholds.

Table 13.273. Register 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0949	3:0	R/W	IN_EN	Enable (or powerdown) the IN3 - IN0 input buffers. 0: Powerdown input buffer 1: Enable and Power-up input buffer
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	Select Pulsed CMOS input buffer for IN3-IN0. See 3.2 Types of Inputs for more information. 0: Standard Input Format 1: Pulsed CMOS Input Format

When a clock input is disabled, it is powered down as well.

- IN0: IN_EN 0x0949[0], IN_PULSED_CMOS_EN 0x0949[4]
- IN1: IN_EN 0x0949[1], IN_PULSED_CMOS_EN 0x0949[5]
- IN2: IN_EN 0x0949[2], IN_PULSED_CMOS_EN 0x0949[6]
- IN3: IN_EN 0x0949[3], IN_PULSED_CMOS_EN 0x0949[7]

Table 13.274. Register 0x094A Input Clock Enable to DSPLL

Reg Address	Bit Field	Type	Name	Description
0x094A	3:0	R/W	INX_TO_PFD_EN	Value calculated in CBPro.

Table 13.275. Register 0x094E–0x094F Input Clock Buffer Hysteresis

Reg Address	Bit Field	Type	Name	Description
0x094E	7:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro.
0x094F	3:0	R/W	REFCLK_HYS_SEL	

Table 13.276. Register 0x094F Input CMOS Threshold Select

Reg Address	Bit Field	Type	Name	Description
0x094F	7:4	R/W	CMOS_HI_THR	CMOS Clock input threshold select for inputs IN3-IN0. 0: Low threshold (Pulsed CMOS) 1: Standard Threshold - Use with DC coupled CMOS input clocks

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Table 13.277. Register 0x0A02 Enable N-divider 0.5x

Reg Address	Bit Field	Type	Name	Description
0x0A02	4:0	R/W	N_ADD_0P5	Value calculated in CBPro.

Table 13.278. Register 0x0A03 Output N Divider to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0A03	4:0	R/W	N_CLK_TO_OUTX_EN	Enable output clocks from N[4:0]. 0: N divider output disabled. 1: N divider output enabled.

Note: In the Si5381, N0 (DSPLL A), N2 (DSPLL C), and N3 (DSPLL D) MUST be enabled when those DSPLLs are active. ClockBuilder Pro determines these values when changing settings for the device.

Table 13.279. Register 0x0A04 Output N Divider Integer Divide Mode

Reg Address	Bit Field	Type	Name	Description
0x0A04	4:0	R/W	N_PIBYP	Bypass fractional divider for N[4:0]. 0: Fractional (or Integer) division - Required for N0, N2, N3. Optional for N1, N4. Recommended when changing settings during operation 1: Integer-only division - best phase noise - Recommended for Si5381 N1, N4 with Integer divisors Note that a device Soft Reset (0x001C[0]=1) must be issued after changing the settings in this register.

Note: In the Si5381, must be set to 0x0 for N0 (DSPLL A), N2 (DSPLL C), and N3 (DSPLL D). Provides a small improvement in phase noise when used with integer N1, N4. ClockBuilder Pro determines these values when changing settings for the device.

Table 13.280. Register 0x0A05 Output N Divider Power Down

Reg Address	Bit Field	Type	Name	Description
0x0A05	4:0	R/W	N_PDNB	Powerdown unused N dividers N[4:0] 0: N divider powered down 1: N divider powered up and enabled

Note: N0 (DSPLL A), N2 (DSPLL C), and N3 (DSPLL D) MUST be enabled when those DSPLLs are active. ClockBuilder Pro determines these values when changing settings for the device.

Table 13.281. Register 0x0A14 Output N0 Divider Auto-Disable

Reg Address	Bit Field	Type	Name	Description
0x0A14	3	R/W	N0_LOAD_AUTO_DIS	Set by CBPro.

Table 13.282. Register 0x0A1A Output N1 Divider Auto-Disable

Reg Address	Bit Field	Type	Name	Description
0x0A1A	3	R/W	N1_LOAD_AUTO_DIS	Set by CBPro.

Table 13.283. Register 0x0A20 Output N2 Divider Auto-Disable

Reg Address	Bit Field	Type	Name	Description
0x0A20	3	R/W	N2_LOAD_AUTO_DIS	Set by CBPro.

Table 13.284. Register 0x0A26 Output N3 Divider Auto-Disable

Reg Address	Bit Field	Type	Name	Description
0x0A26	3	R/W	N3_LOAD_AUTO_DIS	Set by CBPro.

Table 13.285. Register 0x0A2C Output N4 Divider Auto-Disable

Reg Address	Bit Field	Type	Name	Description
0x0A2C	3	R/W	N4_LOAD_AUTO_DIS	Set by CBPro.

13.11 Page B Registers

Table 13.286. Register 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See 2.1.1 Updating Registers During Device Operation for more information.

Table 13.287. Register 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See 2.1.1 Updating Registers During Device Operation for more information.

Table 13.288. Register 0x0B44 Clock Control for Fractional Dividers

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Clock Disable for the fractional divide of the input P dividers. [P3, P2, P1, P0]. Must be set to a 0 if the P divider has a fractional value. 0: Enable the clock to the fractional divide part of the P divider. 1: Disable the clock to the fractional divide part of the P divider.
0x0B44	4	R/W	FRACN_CLK_DIS_PLLA	Clock disable for the fractional divide of the feedback M divider in PLLA. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	5	R/W	FRACN_CLK_DIS_PLLB	Clock disable for the fractional divide of the feedback M divider in PLLB. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	6	R/W	FRACN_CLK_DIS_PLLC	Clock disable for the fractional divide of the feedback M divider in PLLC. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Reg Address	Bit Field	Type	Name	Description
0x0B44	7	R/W	FRACN_CLK_DIS_PLLD	Clock disable for the fractional divide of the feedback M divider in PLLD. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Table 13.289. Register 0x0B45 LOL Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B45	0	R/W	CLK_DIS_PLLA	Disable PLL A LOL clock. Must be 0 for normal LOL operation.
0x0B45	1	R/W	CLK_DIS_PLLB	Disable PLL B LOL clock. Must be 0 for normal LOL operation.
0x0B45	2	R/W	CLK_DIS_PLLC	Disable PLL C LOL clock. Must be 0 for normal LOL operation.
0x0B45	3	R/W	CLK_DIS_PLLD	Disable PLL D LOL clock. Must be 0 for normal LOL operation.

Table 13.290. Register 0x0B46 Loss of Signal Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Disables LOS clock for IN3 - IN0. Must be set to 0 to enable the LOS function of the respective inputs.

ClockBuilder Pro handles these bits when changing settings for all portions of the device.

Table 13.291. Register 0x0B47 DSPLL OOF Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B47	4:0	R/W	OOF_CLK_DIS	Bits 3:0 disable OOF clocks for DSPLLs D:A. Bit 4 disable the OOF clock for the XAXB reference clock. Set to 0 for normal operation.

Table 13.292. Register 0x0B48 DSPLL OOF Divider Disables

Reg Address	Bit Field	Type	Name	Description
0x0B48	4:0	R/W	OOF_DIV_CLK_DIS	Bits 3:0 disable OOF divider for DSPLLs D:A. Bit 4 disable the OOF clock for the XAXB reference clock. Set to 0 for normal operation.

Table 13.293. Register 0x0B49 Reserved Control_2

Reg Address	Bit Field	Type	Name	Description
0x0B49	1:0	R/W	CAL_DIS	Must be 0 for normal operation.

Reg Address	Bit Field	Type	Name	Description
0x0B49	3:2	R/W	CAL_FORCE	Must be 0 for normal operation.

ClockBuilder Pro handles these bits when changing settings for the device.

Table 13.294. Register 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	4:0	R/W	N_CLK_DIS	Disable digital clocks from each DSPLL [1 D C B A] to the N dividers. The most significant bit must always be set to 1. Bits 3:0 must be set to 0 to use the corresponding DSPLL output. See also related registers 0x0A03 and 0x0A05.
0x0B4A	5	R/W	M_CLK_DIS	Disable M divider. Must be set to 0 to enable the M divider.
0x0B4A	6	R/W	M_DIV_CAL_DIS	Disable M divider calibration. Must be set to 0 to allow calibration.

ClockBuilder Pro handles these bits when changing settings for the device.

Table 13.295. Register 0x0B57-0B58 VCO Calcode

Reg Address	Bit Field	Type	Name	Description
0x0B57	7:0	R/W	VCO_RESET_CAL-CODE	Value calculated in CBPro.
0x0B58	3:0	R/W	VCO_RESET_CAL-CODE	

13.12 Page C Registers

Table 13.296. Register 0x0C02 Clock Validation Configuration

Reg Address	Bit Field	Type	Name	Description
0x0C02	2:0	R/W	VAL_DIV_CTL0	Set by CBPro.
0x0C02	4	R/W	VAL_DIV_CTL1	Set by CBPro.

Table 13.297. Register 0x0C03 Clock Validation Configuration

Reg Address	Bit Field	Type	Name	Description
0x0C03	3:0	R/W	IN_CLK_VAL_PWR_UP_DIS	Set by CBPro.

Table 13.298. Register 0x0C07 Clock Validation Configuration

Reg Address	Bit Field	Type	Name	Description
0x0C07	0	R/W	IN_CLK_VAL_EN	Set by CBPro.

Table 13.299. Register 0x0C08 Clock Validation Configuration

Reg Address	Bit Field	Type	Name	Description
0x0C08	7:0	R/W	IN_CLK_VAL_TIME	Set by CBPro.

14. Si5382 Register Map

14.1 Page 0 Registers

Table 14.1. Register 0x0000 Die Rev

Reg Address	Bit Field	Type	Name	Default	Description
0x0000	3:0	R	DIE_REV	0	4-bit die revision number

Table 14.2. Register 0x0001 Page

Reg Address	Bit Field	Type	Name	Default	Description
0x0001	7:0	R/W	PAGE	0	Select one of 256 possible pages.

This is the “Page Register” which is located at address 0x01 on every page. When read, it will indicate the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, etc. See *AN926: Reading and Writing Registers with SPI and I2C for Si534x/8x Devices* for more information on register paging.

Table 14.3. Register 0x0002-0x0003 Base Part Number

Reg Address	Bit Field	Type	Name	Default	Description
0x0002	7:0	R	PN_BASE	0x82	Four-digit ,"base" part number, one nibble per digit. Example: Si5382A-E12346-GM. The base part number (OPN) is 5382, which is stored in this register.
0x0003	15:8	R	PN_BASE	0x53	

See 12.3 Part Numbering Summary for more information on part numbers.

Table 14.4. Register 0x0004 Device Grade

Reg Address	Bit Field	Type	Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed grade. 0 = A, 1 = B, 2 = C, 3 = D, 4 = E, etc. For example in Si5382A-E12346-GM, the GRADE is A = 0

See 12.3 Part Numbering Summary for more information on part numbers. Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 14.5. Register 0x0005 Device Revision

Reg Address	Bit Field	Type	Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B; 2 = C, 3 = D, 4 = E, etc. For example in Si5382A-E12346-GM, the device revision is E = 4

See 12.3 Part Numbering Summary for more information on part numbers. Refer to the device data sheet Ordering Guide section for more information about device grades.

The software tool version that created the register values that are downloaded at power up is represented by TOOL_VERSION.

Table 14.6. Register 0x0009 Temperature Grade

Reg Address	Bit Field	Type	Name	Description
0x0009	7:0	R	TEMP_GRADE	Device temperature grade: 0: Industrial (-40 to 85 °C

See 12.3 Part Numbering Summary for more information on part numbers.

Table 14.7. Register 0x000A Package ID

Reg Address	Bit Field	Type	Name	Description
0x000A	7:0	R	PKG_ID	Package Identifier: 0: 64-pin 9x9 mm QFN

See 12.3 Part Numbering Summary for more information on part numbers.

Table 14.8. Register 0x000B I2C Address

Reg Address	Bit Field	Type	Name	Description
0x000B	6:0	R	I2C_ADDR	7-bit I2C Address

Note that the two least significant bits, [1:0], are determined by the voltages on the A1 and A0 input pins respectively. This setting is not saved as part of the usual NVM write procedure. To update this register in a non-volatile way, the "Si534x8x I2C Address Burn Tool" allows updating this value one time. This utility is included in the ClockBuilder Pro installation and can be accessed under the "Misc" folder in the installation directory.

Table 14.9. Register 0x000C Device Status

Reg Address	Bit Field	Type	Name	Description
0x000C	0	R	SYSINCAL	1 if the device is currently calibrating.
0x000C	1	R	LOSXAXB	1 if there is currently no signal from the XAXB reference clock.
0x000C	2	R	LOSREF	1 if there is currently no signal detected from the XAXB reference clock.
0x000C	3	R	XAXB_ERR	1 if there is currently a problem locking to the XAXB reference clock.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is currently an SMB Bus Timeout error.

See 3.3 Fault Monitoring for more information.

Table 14.10. Register 0x000D Out-of-Frequency (OOF) and Loss-of Signal (LOS) Status

Reg Address	Bit Field	Type	Name	Description
0x000D	3:0	R	LOS	1 if [IN3 - IN0] is currently LOS
0x000D	7:4	R	OOF	1 if [IN3 - IN0] is currently OOF

See 3.3 Fault Monitoring for more information.

- IN0: LOS 0x000D[0], OOF 0x000D[4]
- IN1: LOS 0x000D[1], OOF 0x000D[5]
- IN2: LOS 0x000D[2], OOF 0x000D[6]
- IN3: LOS 0x000D[3], OOF 0x000D[7]

Table 14.11. Register 0x000E Holdover (HOLD) and Loss-of-Lock (LOL) Status

Reg Address	Bit Field	Type	Name	Description
0x000E	1:0	R	LOL_PLL[B:A]	1 if the DSPLL[B:A] is currently out of lock
0x000E	5:4	R	HOLD_PLL[B:A]	1 if the DSPLL[B:A] is currently in Holdover or Freerun

See 3.3 Fault Monitoring for more information.

Table 14.12. Register 0x000F DSPLL Calibration Status

Reg Address	Bit Field	Type	Name	Description
0x000F	5:4	R	CAL_PLL[B:A]	1 if the DSPLL[B:A] internal calibration is currently busy

See 3.3 Fault Monitoring for more information.

Table 14.13. Register 0x0011 Device Status Flags

Reg Address	Bit Field	Type	Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Flag 1 if the device was or is in SYSINCAL
0x0011	1	R/W	LOSXAXB_FLG	Flag 1 if the XAXB reference clock was or is LOSXAXB
0x0011	2	R/W	LOSREF_FLG	Flag 1 if XAXB reference clock was or is LOSREF
0x0011	3	R/W	XAXB_ERR_FLG	Flag 1 if XAXB reference clock was or is XAXB_ERR
0x0011	5	R/W	SMB_TMOUT_FLG	Flag 1 if SMB_TMOUT was or is in error

These are sticky flag bits corresponding to the bits in register 0x000C. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000C register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

Table 14.14. Register 0x0012 OOF and LOS Status Flags

Reg Address	Bit Field	Type	Name	Description
0x0012	3:0	R/W	LOS_FLG	Flag 1 if [IN3 - IN0] was or is LOS
0x0012	7:4	R/W	OOF_FLG	Flag 1 if [IN3 - IN0] was or is OOF

These are sticky flag bits corresponding to the bits in register 0x000D. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000D register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

- IN0: LOS_FLG 0x0012[0], OOF_FLG 0x0012[4]
- IN1: LOS_FLG 0x0012[1], OOF_FLG 0x0012[5]
- IN2: LOS_FLG 0x0012[2], OOF_FLG 0x0012[6]
- IN3: LOS_FLG 0x0012[3], OOF_FLG 0x0012[7]

Table 14.15. Register 0x0013 HOLD and LOL Status Flags

Reg Address	Bit Field	Type	Name	Description
0x0013	1:0	R/W	LOL_FLG_PLL[B:A]	Flag 1 if the DSPLL was or is LOL
0x0013	5:4	R/W	HOLD_FLG_PLL[B:A]	Flag 1 if the DSPLL was or is in Holdover or Freerun

These are sticky flag bits corresponding to the bits in register 0x000E. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000E register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

Table 14.16. Register 0x0014 DSPLL Calibration Status Flag

Reg Address	Bit Field	Type	Name	Description
0x0014	5:4	R/W	CAL_FLG_PLL[B:A]	Flag 1 if the internal calibration was or is busy

These are sticky flag bits corresponding to the bits in register 0x000F. They are cleared by writing 0 to the bit that has been set. The corresponding 0x000F register bit must be 0 to clear this sticky flag bit. See 3.3 Fault Monitoring for more information.

Table 14.17. Register 0x0017 Device Status Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_FLG_MSK	1 to mask LOSXAXB_FLG from causing an interrupt
0x0017	2	R/W	LOSREF_INTR_MSK	1 to mask LOSREF_FLG from causing an interrupt
0x0017	3	R/W	XAXB_ERR_INTR_MSK	1 to mask LOL_FLG from causing an interrupt
0x0017	5	R/W	SMBUS_IMOUT_ FLG_MSK	1 to mask SMBUS_TMOUT_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0011. See 3.3.6 INTRb Interrupt Configuration for more information.

Table 14.18. Register 0x0018 OOF and LOS Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1 to mask LOS_FLG from causing an interrupt
0x0018	7:4	R/W	OOF_INTR_MSK	1 to mask OOF_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0012. See 3.3.6 INTRb Interrupt Configuration for more information.

- IN0: LOS_INTR_MSK 0x0018[0], OOF_INTR_MSK 0x0018[4]
- IN1: LOS_INTR_MSK 0x0018[1], OOF_INTR_MSK 0x0018[5]
- IN2: LOS_INTR_MSK 0x0018[2], OOF_INTR_MSK 0x0018[6]
- IN3: LOS_INTR_MSK 0x0018[3], OOF_INTR_MSK 0x0018[7]

Table 14.19. Register 0x0019 HOLD and LOL Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0019	1:0	R/W	LOL_INTR_MSK_PLL[B:A]	1 to mask LOL_FLG from causing an interrupt
0x0019	5:4	R/W	HOLD_INTR_MSK_PLL[B:A]	1 to mask HOLD_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0013. See 3.3.6 INTRb Interrupt Configuration for more information.

Table 14.20. Register 0x001A PLL In Calibration Interrupt Mask

Reg Address	Bit Field	Type	Name	Description
0x001A	5:4	R/W	CAL_INTR_MSK_PLL[B:A]	1 to mask CAL_FLG from causing an interrupt

These are interrupt mask bits corresponding to the bits in register 0x0014. See 3.3.6 INTRb Interrupt Configuration for more information.

Table 14.21. Register 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Name	Description
0x001C	0	S	SOFT_RST	1 Initializes and calibrates the entire device 0 No effect
0x001C	1	S	SOFT_RST_PLLA	1 Initializes and calibrates DSPLLA 0 No effect
0x001C	2	S	SOFT_RST_PLLB	1 Initializes and calibrates DSPLLB 0 No effect

Soft Reset restarts the device using the existing register values without loading from NVM. Soft Reset also updates registers requiring a separate update strobe, including the DSPLL bandwidth registers as well as the P, M, N, and R dividers. Unlike SOFT_RST_ALL, the SOFT_RST_PLLx bits do not update the loop BW values. If these have changed, the update can be done by writing to BW_UPDATE_PLLA andBW_UPDATE_PLLB, at addresses 0x0414 and 0x0514.

Table 14.22. Register 0x001D FINC, FDEC DCO Controls for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x001D	0	S	FINC	0: No effect 1: A rising edge will cause an frequency increment for DSPLL A when the N_FSTEP_MSK bits are 0.
0x001D	1	S	FDEC	0: No effect 1: A rising edge will cause an frequency decrement for DSPLL A when the N_FSTEP_MSK bits are 0.

Table 14.23. Register 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Name	Description
0x001E	0	R/W	PDN	Place the device into a low current Powerdown state. Note that the serial interface and registers remain active in this state. The DSPLLs will need to re-acquire lock when exiting this state. 0: Normal Operation (default) 1: Powerdown Device
0x001E	1	S	HARD_RST	Perform Hard Reset with NVM read. 0: Normal Operation 1: Hard Reset the device
0x001E	2	S	SYNC	Resets all R dividers. Logically equivalent to asserting the SYNCb pin. 0: Normal Operation 1: Reset R Dividers

Table 14.24. Register 0x0020 DSPLL_SEL[1:0] Control of FINC/FDEC for DCO

Reg Address	Bit Field	Type	Name	Description
0x0020	0	R/W	FSTEP_PLL_SINGLE	0: FSTEP_PLL bits are disabled. 1: DSPLL_SEL[1:0] FSTEP_PLL bits are enabled. See FSTEP_PLL_REGCTRL below.
0x0020	1	R/W	FSTEP_PLL_REGCTRL	Only active when FSTEP_PLL_SINGLE = 1. 0: FSTEP_PLL bits are disabled. 1: FSTEP_PLL bits are enabled.

Reg Address	Bit Field	Type	Name	Description
0x0020	3:2	R/W	FSTEP_PLL[1:0]	Used to select which PLL (M divider) is affected by FINC/FDEC. 0: DSPLL A M-divider 1-3: Reserved

Table 14.25. Register 0x0022 Output Enable Group Controls

Reg Address	Bit Field	Type	Name	Description
0x0022	0	R/W	OE_REG_SEL	Selects between Pin and Register control for output disable. 0: OEb Pin disable (default) 1: OE Register disable
0x0022	1	R/W	OE_REG_DIS	When OE_REG_SEL = 1: 0: Disable selected outputs 1: Enable selected outputs

By default ClockBuilder Pro sets the OEb pin controlling all outputs. OUTALL_DISABLE_LOW (0x0102[0]) must be high (enabled) to allow the OEb pin to enable outputs. Note that the OE_REG_DIS bit (active high) has inverted logic sense from the OEb pin (active low). See 4.7.5 Output Driver Disable Source Summary for more information.

Table 14.26. Register 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Name	Description
0x002B	3	R/W	SPI_3WIRE	Selects operating mode for SPI interface: 0: 4-wire SPI (default) 1: 3-wire SPI

This bit is ignored for I2C bus operation, when I2C_SEL is high. The SPI_3WIRE setting may be updated by either 3-wire or 4-wire writes, since the same 3 pins are used in either mode. When changing this setting the serial interface will be ready to read registers on the next command. 4-wire mode (0x002B=0x0) is the safe default choice to avoid possible contention on the bi-directional 3-wire data pin.

Table 14.27. Register 0x002C LOS Enables

Reg Address	Bit Field	Type	Name	Description
0x002C	3:0	R/W	LOS_EN	Enable LOS detection on IN3 - IN0. 0: Disable LOS Detection 1: Enable LOS Detection
0x002C	4	R/W	LOSXAXB_DIS	Enable LOS detection on the XAXB reference clock. 0: Enable LOS Detection (default). 1: Disable LOS Detection.

- IN0: LOS_EN[0]
- IN1: LOS_EN[1]
- IN2: LOS_EN[2]

- IN3: LOS_EN[3]

Table 14.28. Register 0x002D LOS Clear Delays

Reg Address	Bit Field	Type	Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	IN0 LOS Clear delay. 0: 2 ms 1: 100 ms 2: 200 ms 3: 1000 ms
0x002D	3:2	R/W	LOS1_VAL_TIME	IN1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	IN2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	IN3, same as above

When a valid input clock is not present on the input, LOS will be asserted. When the clock returns, it must remain valid for this period of time before that clock is considered to be qualified again.

Table 14.29. Register 0x002E-0x002F IN0 LOS Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit LOS Trigger Threshold value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value, given a particular frequency plan.

Table 14.30. Register 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit LOS Clear Threshold value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold, given a particular frequency plan.

All 4 input buffers are identical in terms of control. The single set of descriptions for IN0 above also apply to IN1-IN3.

Table 14.31. Output Registers Following the Same Definitions as IN0

Register Addresses	Description	(Same as) Addresses
0x0030 - 0x0031	IN1 LOS Trigger Threshold	0x002E - 0x002F
0x0038 - 0x0039	IN1 LOS Clear Threshold	0x002E - 0x002F
0x0032 - 0x0033	IN2 LOS Trigger Threshold	0x002E - 0x002F
0x003A - 0x003B	IN2 LOS Clear Threshold	0x002E - 0x002F
0x0034 - 0x0035	IN3 LOS Trigger Threshold	0x002E - 0x002F
0x003C - 0x003D	IN3 LOS Clear Threshold	0x002E - 0x002F

Table 14.32. Register 0x003E LOS Min Period Enable

Reg Address	Bit Field	Type	Name	Description
0x003E	7:4	R/W	LOS_MIN_PERI-OD_EN	Values set by CBPro.

Table 14.33. Register 0x003F OOF Enable

Reg Address	Bit Field	Type	Name	Description
0x003F	3:0	R/W	OOF_EN	Enable Precision OOF for IN3 - IN0 0: Disable Precision OOF 1: Enable Precision OOF
0x003F	7:4	R/W	FAST_OOF_EN	Enable Fast OOF for IN3 - IN0 0: Disable Fast OOF 1: Enable Fast OOF

- IN0: OOF_EN[0], FAST_OOF_EN[4]
- IN1: OOF_EN[1], FAST_OOF_EN[5]
- IN2: OOF_EN[2], FAST_OOF_EN[6]
- IN3: OOF_EN[3], FAST_OOF_EN[7]

Table 14.34. Register 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	Select reference 0ppm 0: IN0 1: IN1 2: IN2 3: IN3 4: XAXB reference clock (default) 5-7: Reserved

Table 14.35. Register 0x0041 OOF0 Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0041	4:0	R/W	OOF0_DIV_SEL	Values calculated by CBPro.

Table 14.36. Register 0x0042 OOF1 Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0042	4:0	R/W	OOF1_DIV_SEL	Values calculated by CBPro.

Table 14.37. Register 0x0043 OOF2 Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0043	4:0	R/W	OOF2_DIV_SEL	Values calculated by CBPro.

Table 14.38. Register 0x0044 OOF3 Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0044	4:0	R/W	OOF3_DIV_SEL	Values calculated by CBPro.

Table 14.39. Register 0x0045 OOFXO Divider Select

Reg Address	Bit Field	Type	Name	Description
0x0045	4:0	R/W	OOFXO_DIV_SEL	Values calculated by CBPro.

Table 14.40. Register 0x0046-0x0049 Precision OOF Set Thresholds

Reg Address	Bit Field	Type	Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	Precision OOF Set Threshold. The range is from ±2 ppm to ±510 ppm in 2 ppm steps. Set Threshold (ppm) = OOFx_SET_THR x 2 ppm OOF will be continuously indicated if this is set to 0.
0x0047	7:0	R/W	OOF1_SET_THR	
0x0048	7:0	R/W	OOF2_SET_THR	
0x0049	7:0	R/W	OOF3_SET_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 14.41. Register 0x004A-0x004D Precision OOF Clear Thresholds

Reg Address	Bit Field	Type	Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	Precision OOF Clear Threshold. The range is from ±2 ppm to ±510 ppm in 2 ppm steps. Clear Threshold (ppm) = OOFx_CLR_THR x ±2 ppm Note that OOF will be continuously indicated if this is set to 0.
0x004B	7:0	R/W	OOF1_CLR_THR	
0x004C	7:0	R/W	OOF2_CLR_THR	
0x004D	7:0	R/W	OOF3_CLR_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 14.42. Register 0x004E–0x004F OOF Detection Windows

Reg Address	Bit Field	Type	Name	Description
0x004E	2:0	R/W	FAST_OOF0_DETWIN_SEL	Values calculated by CBPro.
0x004E	6:4	R/W	FAST_OOF1_DETWIN_SEL	
0x004F	2:0	R/W	FAST_OOF2_DETWIN_SEL	
0x004F	6:4	R/W	FAST_OOF3_DETWIN_SEL	

Table 14.43. Register 0x0050 OOF on LOS Controls

Reg Address	Bit Field	Type	Name	Description
0x0050	3:0	R/W	OOF_ON_LOS	Values set by CBPro.

Table 14.44. Register 0x0051-0x0054 Fast OOF Set Thresholds

Reg Address	Bit Field	Type	Name	Description
0x0051	3:0	R/W	FAST_OOF0_SET_THR	Fast OOF Set Threshold. The range is from ±1,000 ppm to ±16,000 ppm in 1000 ppm steps. Fast Set Threshold (ppm) = (FAST_OOFx_SET_THR + 1) x ±1000 ppm Note that OOF will be continuously indicated if this is set to 0.
0x0052	3:0	R/W	FAST_OOF1_SET_THR	
0x0053	3:0	R/W	FAST_OOF2_SET_THR	
0x0054	3:0	R/W	FAST_OOF3_SET_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 14.45. Register 0x0055-0x0058 Fast OOF Clear Thresholds

Reg Address	Bit Field	Type	Name	Description
0x0055	3:0	R/W	FAST_OOF0_CLR_THR	Fast OOF Clear Threshold. The range is from ±1,000 ppm to ±16,000 ppm in 1000 ppm steps. Fast Clear Threshold (ppm) = (FAST_OOFx_CLR_THR + 1) * ±1000ppm Note that OOF will be continuously indicated if this is set to 0.
0x0056	3:0	R/W	FAST_OOF1_CLR_THR	
0x0057	3:0	R/W	FAST_OOF2_CLR_THR	
0x0058	3:0	R/W	FAST_OOF3_CLR_THR	

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 14.46. Register 0x0059 Fast OOF Detection Window

Reg Address	Bit Field	Type	Name	Description
0x0059	1:0	R/W	FAST_OOF0_DETWIN_SEL	Values calculated by CBPro.
0x0059	3:2	R/W	FAST_OOF1_DETWIN_SEL	
0x0059	5:4	R/W	FAST_OOF2_DETWIN_SEL	
0x0059	7:6	R/W	FAST_OOF3_DETWIN_SEL	

Table 14.47. Register 0x005A–0x005D OOF0 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x005A	7:0	R/W	OOF0_RATIO_REF	Values calculated by CBPro.
0x005B	15:8	R/W	OOF0_RATIO_REF	
0x005C	23:16	R/W	OOF0_RATIO_REF	
0x005D	25:24	R/W	OOF0_RATIO_REF	

Table 14.48. Register 0x005E–0x0061 OOF1 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x005E	7:0	R/W	OOF1_RATIO_REF	Values calculated by CBPro.
0x005F	15:8	R/W	OOF1_RATIO_REF	
0x0060	23:16	R/W	OOF1_RATIO_REF	
0x0061	25:24	R/W	OOF1_RATIO_REF	

Table 14.49. Register 0x0062–0x0065 OOF2 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x0062	7:0	R/W	OOF2_RATIO_REF	Values calculated by CBPro.
0x0063	15:8	R/W	OOF2_RATIO_REF	
0x0064	23:16	R/W	OOF2_RATIO_REF	
0x0065	25:24	R/W	OOF2_RATIO_REF	

Table 14.50. Register 0x0066–0x0069 OOF3 Ratio for Reference

Reg Address	Bit Field	Type	Name	Description
0x0066	7:0	R/W	OOF3_RATIO_REF	Values calculated by CBPro.
0x0067	15:8	R/W	OOF3_RATIO_REF	
0x0068	23:16	R/W	OOF3_RATIO_REF	
0x0069	25:24	R/W	OOF3_RATIO_REF	

Table 14.51. Register 0x0092 Fast LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x0092	0	R/W	LOL_FST_EN_PLLA	Fast LOL Enable. Large input frequency errors will quickly assert LOL when enabled. 0: Disable Fast LOL 1: Enable Fast LOL (default)
0x0092	1	R/W	LOL_FST_EN_PLLB	

Table 14.52. Register 0x0093 Fast LOL Detection Window

Reg Address	Bit Field	Type	Name	Description
0x0093	3:0	R/W	LOL_FST_DETWIN_SEL_PLLA	Values calculated by CBPro.
0x0093	7:4	R/W	LOL_FST_DETWIN_SEL_PLLB	

Table 14.53. Register 0x0095 Fast LOL Detection Value

Reg Address	Bit Field	Type	Name	Description
0x0095	1:0	R/W	LOL_FST_VALWIN_SEL_PLLA	Values calculated by CBPro.
0x0095	3:2	R/W	LOL_FST_VALWIN_SEL_PLLB	

Table 14.54. Register 0x0096 Fast LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x0096	3:0	R/W	LOL_FST_SET_THR_SEL_PLLA	Values calculated by CBPro.
0x0096	7:4	R/W	LOL_FST_SET_THR_SEL_PLLB	

Table 14.55. Register 0x0098 Fast LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x0098	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLA	Values calculated by CBPro.
0x0098	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLB	

Table 14.56. Register 0x009A LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x009A	1:0	R/W	LOL_SLOW_EN_PLL[B:A]	Enable LOL detection. 0: LOL Disabled 1: LOL Enabled

See 3.3.3 Input OOF (Out-of-Frequency) Detection for more information.

Table 14.57. Register 0x009B-0x009C Slow LOL Detection Value

Reg Address	Bit Field	Type	Name	Description
0x009B	3:0	R/W	LOL_SLW_DET-WIN_SEL_PLLA	Values calculated by CBPro.
0x009B	7:4	R/W	LOL_SLW_DET-WIN_SEL_PLLB	

Table 14.58. Register 0x009D Slow LOL Detection Value

Reg Address	Bit Field	Type	Name	Description
0x009D	1:0	R/W	LOL_SLW_VAL-WIN_SEL_PLLA	Values calculated by CBPro.
0x009D	3:2	R/W	LOL_SLW_VAL-WIN_SEL_PLLB	

Table 14.59. Register 0x009E LOL Set Threshold

Reg Address	Bit Field	Type	Name	Description
0x009E	3:0	R/W	LOL_SLW_SET_THR_PLLA	LOL Set Threshold.
0x009E	7:4	R/W	LOL_SLW_SET_THR_PLLB	See the list below for settings.

Table 14.60. Register 0x00A0 LOL Clear Threshold

Reg Address	Bit Field	Type	Name	Description
0x00A0	3:0	R/W	LOL_SLW_CLR_THR_PLLA	LOL Clear Threshold.
0x00A0	7:4	R/W	LOL_SLW_CLR_THR_PLLB	See the list below for settings.

LOL_SET_THR and LOL_CLR_THR Threshold settings:

- 0 = ±0.1 ppm
- 1 = ±0.3 ppm
- 2 = ±1 ppm
- 3 = ±3 ppm
- 4 = ±10 ppm
- 5 = ±30 ppm
- 6 = ±100 ppm
- 7 = ±300 ppm
- 8 = ±1000 ppm
- 9 = ±3000 ppm
- 10 = ±10000 ppm
- 11 - 15 Reserved

Table 14.61. Register 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Name	Description
0x00A2	1:0	R/W	LOL_TIM-ER_EN_PLL[B:A]	Enable Delay for LOL Clear. 0: Disable Delay for LOL Clear 1: Enable Delay for LOL Clear

Extends the time after a clock returns or stabilizes before LOL de-asserts.

Table 14.62. Register 0x00A4-0x00B6 LOL Clear Delay

Reg Address	Bit Field	Type	Name	Description
0x00A4	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLA	29-bit value
0x00A5	15:8			
0x00A6	23:16			
0x00A7	28:24			
0x00A9	7:0	R/W	LOL_CLR_DELAY_DIV256_PLLB	29-bit value
0x00AA	15:8			
0x00AB	23:16			
0x00AC	28:24			

The LOL Clear Delay value is set by ClockBuilder Pro based on each frequency plan.

Table 14.63. Register 0x00E2 NVM Active Bank

Reg Address	Bit Field	Type	Name	Description
0x00E2	7:0	R	ACTIVE_NVM_BANK	0x03 when no NVM has been burned 0x0F when 1 NVM bank has been burned 0x3F when 2 NVM banks have been burned When ACTIVE_NVM_BANK = 0x3F, the last bank has already been burned. See 2.1.2 NVM Programming for a detailed description of how to program the NVM.

Table 14.64. Register 0x00E3

Reg Address	Bit Field	Type	Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

See 2.1.2 NVM Programming.

Table 14.65. Register 0x00E4

Reg Address	Bit Field	Type	Name	Description
0x00E4	0	S	NVM_READ_BANK	Set to 1 to initiate NVM copy to registers.

Table 14.66. Register 0x00E5 Fastlock Extend Enable

Reg Address	Bit Field	Type	Name	Description
0x00E5	4	R/W	FASTLOCK_EXTEND_EN_PLLA	Enables FASTLOCK_EXTEND.
0x00E5	5	R/W	FASTLOCK_EXTEND_EN_PLLB	

Table 14.67. Register 0x00E6-0x00E9 FASTLOCK_EXTEND_PLLA

Reg Address	Bit Field	Type	Name	Description
0x00E6	7:0	R/W	FASTLOCK_EXTEND_PLLA	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00E7	15:8	R/W	FASTLOCK_EXTEND_PLLA	
0x00E8	23:16	R/W	FASTLOCK_EXTEND_PLLA	
0x00E9	28:24	R/W	FASTLOCK_EXTEND_PLLA	

Table 14.68. Register 0x00EA-0x00ED FASTLOCK_EXTEND_PLLB

Reg Address	Bit Field	Type	Name	Description
0x00EA	7:0	R/W	FSTLK_TIMER_EXT_PLLB	29-bit value. Set by CBPro to minimize the phase transients when switching the PLL bandwidth. See FASTLOCK_EXTEND_SCL_PLLx.
0x00EB	15:8	R/W	FSTLK_TIMER_EXT_PLLB	
0x00EC	23:16	R/W	FSTLK_TIMER_EXT_PLLB	
0x00ED	28:24	R/W	FSTLK_TIMER_EXT_PLLB	

Table 14.69. Register 0x00FE Device Ready

Reg Address	Bit Field	Type	Name	Description
0x00FE	7:0	R	DEVICE_READY	Device Ready indicator. 0x0F: Device is Ready 0xF3: Device is Not ready

Read-only byte to indicate when the device is ready to accept serial bus writes. The user can poll this byte starting at power-up. When reads from DEVICE_READY return 0x0F the user can safely read or write to all registers. Generally, this is only needed after POR, Hard Reset, or after initiating an NVM write. This “Device Ready” register is available on every page in the device at the second to the

last serial address, 0xFE. For example, there is a device ready register at 0x00FE, 0x01FE, 0x02FE, 0x03FE, etc. Since this register is accessible on every page, you should not write the page register when reading DEVICE_READY.

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Table 14.70. Register 0x0102 Global Output Gating for all Clock Outputs

Reg Address	Bit Field	Type	Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	Enable/Disable All output drivers. If the OEb pin is held high, then all outputs will be disabled regardless of this setting. 0: Disable All outputs (default) 1: Enable All outputs

Table 14.71. Register 0x0103 OUT0A Output Enable and R0A Divider Configuration

Reg Address	Bit Field	Type	Name	Description
0x0103	0	R/W	OUT0A_PDN	Powerdown output driver. 0: Normal Operation (default) 1: Powerdown output driver When powered down, outputs pins will be high impedance with a light pull down effect.
0x0103	1	R/W	OUT0A_OE	Enable/Disable individual output. 0: Disable output (default) 1: Enable output
0x0103	2	R/W	OUT0A_RDIV_FORCE	Force R0A output divider divide-by-2. 0: R0A_REG sets divide value (default) 1: Divide value forced to divide-by-2
0x0103	3	R/W	OUT0A_DIV2_BYP	Output divide-by-2 bypass. 0: Use output divide-by-2 (default) 1: Disable output divide-by-2

Setting R0A_REG=0 will not set the divide value to divide-by-2 automatically. OUT0A_RDIV_FORCE must be also be set to a value of 1 to force R0A to divide-by-2. Note that the R0A_REG value will be ignored while OUT0A_RDIV_FORCE=1. See R0A_REG registers, 0x0247-0x0249, for more information. Note that setting OUTx_DIV2_BYP = 1, the output clock duty cycle will be set by the N output divider value.

Table 14.72. Register 0x0104 OUT0A Output Format and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0104	2:0	R/W	OUT0A_FORMAT	Select output format. 0: Reserved 1: Differential Normal mode 2: Differential Low-Power mode 3: Reserved 4: LVCMOS single ended 5: LVCMOS (OUTx pin only) 6: LVCMOS (OUTxb pin only) 7: Reserved
0x0104	3	R/W	OUT0A_SYNC_EN	Synchronous Enable/Disable selection. 0: Asynchronous Enable/Disable (default) 1: Synchronous Enable/Disable (Glitchless)
0x0104	5:4	R/W	OUT0A_DIS_STATE	Determines the logic state of the output driver when disabled: 0: Disable logic Low 1: Disable logic High 2-3: Reserved
0x0104	7:6	R/W	OUT0A_CMOS_DRV	LVCMOS output impedance selection. See 4.6.2 LVCMOS Output Impedance and Drive Strength Selection for valid selections.

Table 14.73. Register 0x0105 Output OUT0A Differential Amplitude and Common Mode

Reg Address	Bit Field	Type	Name	Description
0x0105	3:0	R/W	OUT0A_CM	OUT0A Common Mode Voltage selection. Only applies when OUT0A_FORMAT=1 or 2.
0x0105	6:4	R/W	OUT0A_AMPL	OUT0A Differential Amplitude setting. Only applies when OUT0A_FORMAT=1 or 2.

ClockBuilder Pro is used to select the correct settings for this register. See Table 4.7 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML on page 45 and 15. Appendix—Custom Differential Amplitude Controls for details of the settings.

Table 14.74. Register 0x0106 Output OUT0A Source Selection and LVCMOS Inversion

Reg Address	Bit Field	Type	Name	Description
0x0106	2:0	R/W	OUT0A_MUX_SEL	OUT0A output source divider select. 0: DSPLL A is the source for OUT0A 1: DSPLLB/N1 is the source for OUT0A 2: DSPLLB/N2 is the source for OUT0A 3: DSPLLB/N3 is the source for OUT0A 4: DSPLLB/N4 is the source for OUT0A 5-7: Reserved
0x0106	3	R/W	OUT0A_VDD_SEL_EN	Output Driver VDD Select Enable. Set to 1 for normal operation.
0x0106	5:4	R/W	OUT0A_VDD_SEL	Output Driver VDD Select. 0: 3.3 V 1: 1.8 V 2: 2.5 V 3: Reserved
0x0106	7:6	R/W	OUT0A_INV	OUT0A output LVCMOS inversion. Only applies when OUT0A_FORMAT = 4. See 4.6.4 LVCMOS Output Polarity for more information.

The OUTx_MUX_SEL settings should match the corresponding OUTx_DIS_SRC selections. Note that the setting codes for OUTx_DIS_SRC and OUTx_MUX_SEL are different when selecting the same DSPLL and N-divider.

All output drivers are identical in terms of control. The single set of descriptions above for OUT0A also applies to OUT0-OUT9A:

Table 14.75. Register 0x0107 Output Disable Source DSPLL

Reg Address	Bit Field	Type	Name	Description
0x0107	2:0	R/W	OUT0A_DIS_SRC	Output clock Squelched (temporary disable) on DSPLL Soft Reset: 0: Reserved 1: DSPLL A squelches output 2: DSPLL B squelches output 3-7: Reserved

The CLKx_DIS_SRC settings should match the corresponding OUTx_MUX_SEL selections. Note that the setting codes for OUTx_DIS_SRC and OUTx_MUX_SEL are different when selecting the same DSPLL.

Table 14.76. Output Registers Following the Same Definitions as OUT0A

Register Address	Description	(Same as) Address
0x0108	OUT0 Powerdown, Output Enable, and R0 Divide-by-2	0x0103
0x0109	OUT0 Signal Format and Configuration	0x0104
0x010A	OUT0 Differential Amplitude and Common Mode	0x0105
0x010B	OUT0 Source Selection and LVCMOS Inversion	0x0106
0x010C	OUT0 Disable Source	0x0107
0x010D	OUT1 Powerdown, Output Enable, and R1 Divide-by-2	0x0103
0x010E	OUT1 Signal Format and Configuration	0x0104
0x010F	OUT1 Differential Amplitude and Common Mode	0x0105
0x0110	OUT1 Source Selection and LVCMOS Inversion	0x0106
0x0111	OUT1 Disable Source	0x0107
0x0112	OUT2 Powerdown, Output Enable, and R2 Divide-by-2	0x0103
0x0113	OUT2 Signal Format and Configuration	0x0104
0x0114	OUT2 Differential Amplitude and Common Mode	0x0105
0x0115	OUT2 Source Selection and LVCMOS Inversion	0x0106
0x0116	OUT2 Disable Source	0x0107
0x0117	OUT3 Powerdown, Output Enable, and R3 Divide-by-2	0x0103
0x0118	OUT3 Signal Format and Configuration	0x0104
0x0119	OUT3 Differential Amplitude and Common Mode	0x0105
0x011A	OUT3 Source Selection and LVCMOS Inversion	0x0106
0x011B	OUT3 Disable Source	0x0107
0x011C	OUT4 Powerdown, Output Enable, and R4 Divide-by-2	0x0103
0x011D	OUT4 Signal Format and Configuration	0x0104
0x011E	OUT4 Differential Amplitude and Common Mode	0x0105
0x011F	OUT4 Source Selection and LVCMOS Inversion	0x0106
0x0120	OUT4 Disable Source	0x0107
0x0121	OUT5 Powerdown, Output Enable, and R5 Divide-by-2	0x0103
0x0122	OUT5 Signal Format and Configuration	0x0104
0x0123	OUT5 Differential Amplitude and Common Mode	0x0105
0x0124	OUT5 Source Selection and LVCMOS Inversion	0x0106
0x0125	OUT5 Disable Source	0x0107
0x0126	OUT6 Powerdown, Output Enable, and R6 Divide-by-2	0x0103
0x0127	OUT6 Signal Format and Configuration	0x0104
0x0128	OUT6 Differential Amplitude and Common Mode	0x0105
0x0129	OUT6 Source Selection and LVCMOS Inversion	0x0106
0x012A	OUT6 Disable Source	0x0107

Register Address	Description	(Same as) Address
0x012B	OUT7 Powerdown, Output Enable, and R7 Divide-by-2	0x0103
0x012C	OUT7 Signal Format and Configuration	0x0104
0x012D	OUT7 Differential Amplitude and Common Mode	0x0105
0x012E	OUT7 Source Selection and LVCMOS Inversion	0x0106
0x012F	OUT7 Disable Source	0x0107
0x0130	OUT8 Powerdown, Output Enable, and R8 Divide-by-2	0x0103
0x0131	OUT8 Signal Format and Configuration	0x0104
0x0132	OUT8 Differential Amplitude and Common Mode	0x0105
0x0133	OUT8 Source Selection and LVCMOS Inversion	0x0106
0x0134	OUT8 Disable Source	0x0107
0x0135	OUT9 Powerdown, Output Enable, and R9 Divide-by-2	0x0103
0x0136	OUT9 Signal Format and Configuration	0x0104
0x0137	OUT9 Differential Amplitude and Common Mode	0x0105
0x0138	OUT9 Source Selection and LVCMOS Inversion	0x0106
0x0139	OUT9 Disable Source	0x0107
0x013A	OUT9A Powerdown, Output Enable, and R9A Divide-by-2	0x0103
0x013B	OUT9A Signal Format and Configuration	0x0104
0x013C	OUT9A Differential Amplitude and Common Mode	0x0105
0x013D	OUT9A Source Selection and LVCMOS Inversion	0x0106
0x013E	OUT9A Disable Source	0x0107

Table 14.77. Register 0x013F-0x0140 Output Force Enable

Reg Address	Bit Field	Type	Name	Description
0x013F	7:0	R/W	OUTX_ALWAYS_ON	Force output driver to remain active, even when fault conditions are present. Used primarily for ZDM. 0: Normal output driver enable/disable (default) 1: Force driver always active (ZDM) [OUT6, OUT5, ..., OUT0, OUT0A]
0x0140	3:0	R/W	OUTX_ALWAYS_ON	[OUT9A, OUT9, OUT8, OUT7]

Table 14.78. Register 0x0141 Output Disable Mask for LOSXAXB

Reg Address	Bit Field	Type	Name	Description
0x0141	1	R/W	OUT_DIS_MSK	Mask alarms from disabling all output drivers. 0: Disable All output drivers on alarm (default) 1: Ignore alarms for output driver disable

Reg Address	Bit Field	Type	Name	Description
0x0141	6	R/W	OUT_DIS_LOSXAXB_MSK	Mask LOSXAXB from disabling all output drivers. 0: Disable All output drivers on LOSXAXB (default) 1: Ignore LOSXAXB for output driver disable

See 4.7.5 Output Driver Disable Source Summary for more information.

Table 14.79. Register 0x0142 Output Disable Mask for LOL

Reg Address	Bit Field	Type	Name	Description
0x0142	1:0	R/W	OUT_DIS_MASK_LOL_PLL[B:A]	Mask LOL from disabling all output drivers. 0: Disable All output drivers on LOL (default) 1: Ignore LOL for output driver disable

See 4.7.5 Output Driver Disable Source Summary for more information.

Table 14.80. Register 0x0145 Output Power Down All

Reg Address	Bit Field	Type	Name	Description
0x0145	0	R/W	OUT_PDN_ALL	Powerdown all output drivers. 0: Normal Operation (default) 1: Powerdown all output drivers

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Table 14.81. Register 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8			
0x020A	23:16			
0x020B	31:24			
0x020C	39:32			
0x020D	47:40			

Table 14.82. Register 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8			
0x0210	23:16			
0x0211	31:24			

The P input divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. The new register values for the P divider will not take effect until the appropriate Px_UPDATE strobe is set as described below.

Note: This ratio of (Px_NUM / Px_DEN) MUST also be an integer when used with DSPLL B.

Table 14.83. Registers that Follow the P0_NUM and P0_DEN Above

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2 Divider Denominator	32-bit Integer Number	0x020E-0x0211
0x0226-0x022B	P3 Divider Numerator	48-bit Integer Number	0x0208-0x020D
0x022C-0x022F	P3 Divider Denominator	32-bit Integer Number	0x020E-0x0211

Table 14.84. Register 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Name	Description
0x0230	0	S	P0_UPDATE	Set these bits for IN3 - IN0 to 1 to latch in new P-divider values. A device Soft Reset (0x001C[0]=1) will also latch in the new values.
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

The Px_UPDATE bit must be asserted to update the internal P divider numerator and denominator values. These update bits are provided in a single register so that all of the P input dividers can be changed at the same time.

Table 14.85. Register P0 Factional Division Enable

Reg Address	Bit Field	Type	Name	Description
0x0231	3:0	R/W	P0_FRACN_MODE	P0 (IN0) input divider fractional mode. Must be set to 0xB for proper operation.
0x0231	4	R/W	P0_FRAC_EN	P0 (IN0) input divider fractional enable. 0: Integer-only division. 1: Fractional (or Integer) division.

Table 14.86. Register P1 Factional Division Enable

Reg Address	Bit Field	Type	Name	Description
0x0232	3:0	R/W	P1_FRACN_MODE	P1 (IN1) input divider fractional mode. Must be set to 0xB for proper operation.
0x0232	4	R/W	P1_FRAC_EN	P1 (IN1) input divider fractional enable. 0: Integer-only division. 1: Fractional (or Integer) division.

Table 14.87. Register P2 Factional Division Enable

Reg Address	Bit Field	Type	Name	Description
0x0233	3:0	R/W	P2_FRACN_MODE	P2 (IN2) input divider fractional mode. Must be set to 0xB for proper operation.
0x0233	4	R/W	P2_FRAC_EN	P2 (IN2) input divider fractional enable. 0: Integer-only division. 1: Fractional (or Integer) division.

Table 14.88. Register P3 Factional Division Enable

Reg Address	Bit Field	Type	Name	Description
0x0234	3:0	R/W	P3_FRACN_MODE	P3 (IN3) input divider fractional mode. Must be set to 0x0B for proper operation
0x0234	4	R/W	P3_FRAC_EN	P3 (IN3) input divider fractional enable. 0: Integer-only division. 1: Fractional (or Integer) division.

Table 14.89. Register 0x0235–0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number.
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	47:40	R/W	MXAXB_NUM	

Changing this register during operation may cause indefinite loss of lock unless the guidelines in Section 2.1.1 Updating Registers During Device Operation. Operation are followed. Either MXAXB_UPDATE or SOFT_RST must be set to cause these changes to take effect.

Table 14.90. Register 0x023B–0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number.
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

Changing this register during operation may cause indefinite loss of lock unless the guidelines in Section 2.1.1 Updating Registers During Device Operation. Operation are followed. Either MXAXB_UPDATE or SOFT_RST must be set to cause these changes to take effect.

Table 14.91. Register 0x023F MXAXB Update

Reg Address	Bit Field	Type	Name	Description
0x023F	1	S	MXAXB_UPDATE	Set to 1 to update the MXAXB_NUM and MXAXB_DEN values. A SOFT_RST may also be used to update these values.

Table 14.92. Register 0x0247-0x0249 R0A Divider

Reg Address	Bit Field	Type	Name	Description
0x0247	7:0	R/W	R0A_REG	24-bit integer final R0A divider selection. R Divisor = (R0A_REG + 1) x 2 However, note that setting R0A_REG = 0 will not set the output to divide-by-2. See notes below.
0x0248	15:8			
0x0249	23:16			

The final output R dividers are even-numbered dividers beginning with divide-by-2. While all other values follow the formula in the bit description above, divide-by-2 requires an extra bit to be set. For divide-by-2, also set OUT0_RDIV_FORCE=1. See the description for register bit 0x0103[2] in this register map.

The R0-R9A dividers follow the same format as the R0A divider description above.

Table 14.93. Registers that Follow the R0A_REG

Register Address	Description	Size	Same as Address
0x024A-0x024C	R0_REG	24-bit Integer Number	0x0247-0x0249
0x024D-0x024F	R1_REG	24-bit Integer Number	0x0247-0x0249
0x0250-0x0252	R2_REG	24-bit Integer Number	0x0247-0x0249
0x0253-0x0255	R3_REG	24-bit Integer Number	0x0247-0x0249
0x0256-0x0258	R4_REG	24-bit Integer Number	0x0247-0x0249
0x0259-0x025B	R5_REG	24-bit Integer Number	0x0247-0x0249
0x025C-0x025E	R6_REG	24-bit Integer Number	0x0247-0x0249
0x025F-0x0261	R7_REG	24-bit Integer Number	0x0247-0x0249
0x0262-0x0264	R8_REG	24-bit Integer Number	0x0247-0x0249
0x0265-0x0267	R9_REG	24-bit Integer Number	0x0247-0x0249
0x0268-0x026A	R9A_REG	24-bit Integer Number	0x0247-0x0249

Table 14.94. Register 0x026B-0x0272 User Design Identifier

Reg Address	Bit Field	Type	Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by the ClockBuilder Pro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, "ULT. 1A" with null character padding sets: • DESIGN_ID0: 0x55 • DESIGN_ID1: 0x4C • DESIGN_ID3: 0x2E • DESIGN_ID4: 0x31 • DESIGN_ID5: 0x41 • DESIGN_ID6: 0x00 • DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 14.95. Register 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: Si5382A-E12346-GM, 12346 is the OPN unique identifier, which sets: • OPN_ID0: 0x31 • OPN_ID1: 0x32 • OPN_ID2: 0x33 • OPN_ID3: 0x34 • OPN_ID4: 0x36
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

See 12.3 Part Numbering Summary for more information on part numbers.

Table 14.96. Registers 0x028A - 0x028D OOFx_TRG_THR_EXT Controls

Reg Address	Type	Name	Description
0x028A[4:0]	R/W	OOF0_TRG_THR_EXT	Set by CBPro.
0x028B[4:0]	R/W	OOF1_TRG_THR_EXT	Set by CBPro.
0x028C[4:0]	R/W	OOF2_TRG_THR_EXT	Set by CBPro.
0x028D[4:0]	R/W	OOF3_TRG_THR_EXT	Set by CBPro.

Table 14.97. Registers 0x028E - 0x0291 OOFx_CLR_THR_EXT Controls

Reg Address	Type	Name	Description
0x028E[4:0]	R/W	OOF0_CLR_THR_EXT	Set by CBPro.
0x028F[4:0]	R/W	OOF1_CLR_THR_EXT	Set by CBPro.
0x0290[4:0]	R/W	OOF2_CLR_THR_EXT	Set by CBPro.
0x0291[4:0]	R/W	OOF3_CLR_THR_EXT	Set by CBPro.

Table 14.98. Register 0x0292 OOF Stop on LOS Controls

Reg Address	Bit Field	Type	Name	Description
0x0292	3:0	R/W	OOF_STOP_ON_LOS	Values set by CBPro.

Table 14.99. Register 0x0293 OOF Clear on LOS Controls

Reg Address	Bit Field	Type	Name	Description
0x0293	3:0	R/W	OOF_CLEAR_ON_LOS	Values set by CBPro.

Table 14.100. Register 0x0294 Fastlock Extend Scale

Reg Address	Bit Field	Type	Name	Description
0x0294	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLA	Scales LOLB_INT_TIMER_DIV256. Set by CBPro.
0x0294	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLB	

Table 14.101. Register 0x0296 Fastlock Delay on Input Switch

Reg Address	Bit Field	Type	Name	Description
0x0296	0	R/W	LOL_SLW_VALWIN_SELX_PLLA	Set by CBPro.
0x0296	1	R/W	LOL_SLW_VALWIN_SELX_PLLB	

Table 14.102. Register 0x0297 Fastlock Delay on Input Switch

Reg Address	Bit Field	Type	Name	Description
0x0297	0	R/W	FAST-LOCK_DLY_ONSW_EN_PLLA	Set by CBPro.
0x0297	1	R/W	FAST-LOCK_DLY_ONSW_EN_PLLB	

Table 14.103. Register 0x0299 Fastlock Delay on LOL Enable

Reg Address	Bit Field	Type	Name	Description
0x0299	0	R/W	FASTLOCK_DLY_ON-LOL_EN_PLLA	Set by CBPro.
0x0299	1	R/W	FASTLOCK_DLY_ON-LOL_EN_PLLB	

Table 14.104. Register 0x029A–0x029C Fastlock Delay on LOLA

Reg Address	Bit Field	Type	Name	Description
0x029A	7:0	R/W	FASTLOCK_DLY_ON-LOL_PLLA	Set by CBPro.
0x029B	15:8	R/W	FASTLOCK_DLY_ON-LOL_PLLA	
0x029C	19:16	R/W	FASTLOCK_DLY_ON-LOL_PLLA	

Table 14.105. Register 0x029D–0x029F Fastlock Delay on LOLB

Reg Address	Bit Field	Type	Name	Description
0x029D	7:0	R/W	FASTLOCK_DLY_ON-LOL_PLLB	Set by CBPro.
0x029E	15:8	R/W	FASTLOCK_DLY_ON-LOL_PLLB	
0x029F	19:16	R/W	FASTLOCK_DLY_ON-LOL_PLLB	

Table 14.106. Register 0x02A6–0x02A8 Fastlock Delay on Input Switch PLLA

Reg Address	Bit Field	Type	Name	Description
0x02A6	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLA	20-bit value. Set by CBPro.
0x02A7	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLA	
0x02A8	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLA	

Table 14.107. Register 0x02A9–0x02AB Fastlock Delay on Input Switch PLLB

Reg Address	Bit Field	Type	Name	Description
0x02A9	7:0	R/W	FAST-LOCK_DLY_ONSW_PLLB	20-bit value. Set by CBPro.
0x02AA	15:8	R/W	FAST-LOCK_DLY_ONSW_PLLB	
0x02AB	19:16	R/W	FAST-LOCK_DLY_ONSW_PLLB	

Table 14.108. Register 0x02B7 LOL Delay from LOS

Reg Address	Bit Field	Type	Name	Description
0x02B7	1:0	R/W	LOL_NO-SIG_TIME_PLLA	Set by CBPro.
0x02B7	3:2	R/W	LOL_NO-SIG_TIME_PLLB	

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Table 14.109. Register 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Name	Description
0x0302	7:0	R/W	N0_NUM	N Output Divider Numerator. 44-bit Integer
0x0303	15:8			
0x0304	23:16			
0x0305	31:24			
0x0306	39:32			
0x0307	43:40			

Table 14.110. Register 0x0308-0x030B N0 Denominator

Reg Address	Bit Field	Type	Name	Description
0x0308	7:0	R/W	N0_DEN	N Output Divider Denominator. 32-bit Integer
0x0309	15:8			
0x030A	23:16			
0x030B	31:24			

The N output divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. Note that this ratio of Nx_NUM / Nx_DEN should also be an integer for best performance. The N output dividers feed into the final output R dividers through the output crosspoint.

Table 14.111. Register 0x030C N0 Update

Reg Address	Bit Field	Type	Name	Description
0x030C	0	S	N0_UPDATE	Set this bit to 1 to latch the N output divider registers into operation.

Setting this self-clearing bit to 1 latches the new N output divider register values into operation. An individual or device Soft Reset will have the same effect.

Table 14.112. Registers that Follow the N0_NUM and N0_DEN Definitions

Register Address	Description	Size	Same as Address
0x030D-0x0312	N1_NUM	44-bit Integer	0x0302-0x0307
0x0313-0x0316	N1_DEN	32-bit Integer	0x0308-0x030B
0x0317	N1_UPDATE	one bit	0x030C
0x0318-0x031D	N2_NUM	44-bit Integer	0x0302-0x0307
0x031E-0x0321	N2_DEN	32-bit Integer	0x0308-0x030B
0x0322	N2_UPDATE	one bit	0x030C
0x0323-0x0328	N3_NUM	44-bit Integer	0x0302-0x0307
0x0329-0x032C	N3_DEN	32-bit Integer	0x0308-0x030B
0x032D	N3_UPDATE	one bit	0x030C

Register Address	Description	Size	Same as Address
0x032E-0x0333	N4_NUM	44-bit Integer	0x0302-0x0307
0x0334-0x0337	N4_DEN	32-bit Integer	0x0308-0x030B
0x0338	N4_UPDATE	one bit	0x030C

Table 14.113. Register 0x0338 Global N Divider Update

Reg Address	Bit Field	Type	Name	Description
0x0338	1	S	N_UPDATE_ALL	Writing a 1 to this bit will update the N output divider values. When this bit is written to 1, all other bits in this register must be written as zeros.

This bit is provided so that all of the N divider values can be changed at the same time. First, write all of the new values to Nx_NUM and Nx_DEN, then set the update bit to 1.

Note: If the intent is to write to the N_UPDATE_ALL to have all Nx dividers update at the same time then make sure only bit 1 N_UPDATE_ALL bit gets set in this register.

Table 14.114. Register 0x0339 DCO FINC/FDEC Control Mask

Reg Address	Bit Field	Type	Name	Description
0x0339	0	R/W	N_FSTEP_MSK_PLLA	DSPLL A DCO control mask 0: Enable FINC/FDEC updates (default) 1: Disable FINC/FDEC updates

Table 14.115. Register 0x033B-0x0340 DCO Step Size for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x033B	7:0	R/W	N0_FSTEPW	44-bit Integer Number.
0x033C	15:8	R/W	N0_FSTEPW	
0x033D	23:16	R/W	N0_FSTEPW	
0x033E	31:24	R/W	N0_FSTEPW	
0x033F	39:32	R/W	N0_FSTEPW	
0x0340	43:40	R/W	N0_FSTEPW	

Table 14.116. Register 0x035B-0x035C N1 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035B-0x035C	7:0	R/W	N1_DELAY[15:8]	8.8-bit, 2s-complement delay for N1

N1_DELAY[7:0] is an 8.8-bit 2's-complement number that sets the output delay of the N1 divider. ClockBuilder Pro calculates the correct value for this register. A Soft Reset of the device, SOFT_RST (0x001C[0] = 1), required to latch in the new delay value(s). Note that the least significant byte (0x035B) is ignored when the N1 divider is in integer mode.

t_{DLY} = Nx_DELAY / 256 x 67.8 ps

f_{VCO}=14.7456 GHz, 1/f_{VCO}=67.8 ps

Table 14.117. Register 0x035D-0x035E N2 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035D-0x035E	7:0	R/W	N2_DELAY[15:8]	8. 8-bit, 2s-complement delay for N2

N2_DELAY behaves in the same manner as N1_DELAY above.

Table 14.118. Register 0x035F-0x0360 N3 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035F-0x0360	7:0	R/W	N3_DELAY[15:8]	8.8-bit, 2s-complement delay for N3

N3_DELAY behaves in the same manner as N1_DELAY above.

Table 14.119. Register 0x0361-0x0362 N4 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0361-0x0362	7:0	R/W	N4_DELAY[15:8]	8.8-bit, 2s-complement delay for N4

N4_DELAY behaves in the same manner as N1_DELAY above.

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Table 14.120. Register 0x0407 Input Selection for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0407	7:6	R	IN_ACTV_PLLA	Currently selected DSPLL A input clock. 0: IN0 1: IN1 2: IN2 3: IN3

This register displays the currently selected input for the DSPLL. In manual select mode, this reflects either the register value or the voltages on the IN_SEL1 and IN_SEL0 pins. In automatic switching mode, it reflects the input currently chosen by the automatic algorithm. If there are no valid input clocks in the automatic mode, this value will retain its previous value until a valid input clock is presented. Note that this value is not meaningful in Holdover or Freerun modes.

Table 14.121. Register 0x0408-0x040D DSPLL Loop Bandwidth for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0408	7:0	R/W	BW0_PLLA	DSPLL A loop bandwidth parameters.
0x0409	7:0	R/W	BW1_PLLA	
0x040A	7:0	R/W	BW2_PLLA	
0x040B	7:0	R/W	BW3_PLLA	
0x040C	7:0	R/W	BW4_PLLA	
0x040D	7:0	R/W	BW5_PLLA	

This group of registers determines the DSPLL A loop bandwidth. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that individual SOFT_RST_PLLA (0x001C[1]) does not update the bandwidth parameters.

Table 14.122. Register 0x040E-0x0413 DSPLL Fastlock Loop Bandwidth for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x040E	7:0	R/W	FAST-LOCK_BW0_PLLA	DSPLL A Fastlock Bandwidth parameters.
0x040F	7:0	R/W	FAST-LOCK_BW1_PLLA	
0x0410	7:0	R/W	FAST-LOCK_BW2_PLLA	
0x0411	7:0	R/W	FAST-LOCK_BW3_PLLA	
0x0412	7:0	R/W	FAST-LOCK_BW4_PLLA	
0x0413	7:0	R/W	FAST-LOCK_BW5_PLLA	

This group of registers determines the DSPLL Fastlock bandwidth. In ClockBuilder Pro, it is selectable from 200 Hz to 4 kHz in factors of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that individual SOFT_RST_PLLA (0x001C[1]) does not update the bandwidth parameters.

Table 14.123. Register 0x0414 DSPLL Bandwidth Update for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0414	0	S	BW_UPDATE_PLLA	Set to 1 to latch updated BWx_PLLA and FAST_BWx_PLLA bandwidth registers into operation.

Setting this self-clearing bit high latches all of the new DSPLL A bandwidth register values into operation. Asserting this strobe will update all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA bandwidths at the same time. A device Soft Reset (0x001C[0]) will have the same effect, but individual DSPLL soft resets will not update these values.

Table 14.124. Register 0x0415-0x041B M Feedback Divider Numerator, 56-bits for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0415	7:0	R/W	M_NUM_PLLA	M feedback divider Numerator 56-bit Integer
0x0416	15:8			
0x0417	23:16			
0x0418	31:24			
0x0419	39:32			
0x041A	47:40			
0x041B	55:48			

Table 14.125. Register 0x041C-0x041F M Feedback Divider Denominator, 32-bits for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x041C	7:0	R/W	M_DEN_PLLA	M feedback divider Denominator 32-bit Integer
0x041D	15:8			
0x041E	23:16			
0x041F	31:24			

The DSPLL M feedback divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. An Integer ratio of (M_NUM / M_DEN) will give the best phase noise performance.

Table 14.126. Register 0x0420 M Divider Update for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0420	0	S	M_UPDATE_PLLA	Set this bit to latch the M feedback divider register values into operation.

Setting this self-clearing bit high latches the new M feedback divider register values into operation. A Soft Reset will have the same effect.

Table 14.127. Register 0x0421 A M Divider Fractional Enable for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0421	3:0	R/W	M_FRAC_MODE_PLLA	M feedback divider fractional mode. Must be set to 0xB for proper operation
0x0421	4	R/W	M_FRAC_EN_PLLA	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0421	5	R/W	Reserved	Must be set to 1 for DSPLL A

Table 14.128. Register 0x0422 A M Divider DSO Step Mask for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0422	0	R/W	M_FSTEPW_MASK_PLLA	M feedback divider DCO mask 0: Enable FINC/FDEC Updates (default) 1: Disable FINC/FDEC Updates

Table 14.129. Register 0x0423-0x0429 M Divider DCO FSTEPW for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0423	7:0	R/W	M_FSTEPW_PLLA	56-bit number
0x0424	15:8			
0x0425	23:16			
0x0426	31:24			
0x0427	39:32			
0x0428	47:40			
0x0429	55:48			

Table 14.130. Register 0x042A Input Clock Select for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x042A	2:0	R/W	IN_SEL_PLLA	Manual Input Select selection (Non-ZDM). 0: IN0 (default), 1: IN1, 2: IN2, 3: IN3 4-7: Reserved

Input clock selection for manual register based and pin controlled clock selection.

Note: When IN_SEL_REGCTRL is low, IN_SEL does not do anything and the clock selection is pin controlled.

Table 14.131. Register 0x042B Fastlock Control for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x042B	0	R/W	FASTLOCK_AUTO_EN_PLLA	Auto Fastlock Enable/Disable. 0: Disable Auto Fastlock (default) 1: Enable Auto Fastlock
0x042B	1	R/W	FASTLOCK_MAN_PLLA	Manually Force Fastlock. 0: Normal Operation (default) 1: Force Fastlock

When Fastlock is enabled by either manual or automatic means, the higher Fastlock bandwidth will be used to provide faster settling of the DSPLL. With FASTLOCK_MAN_PLLA=0 and FASTLOCK_AUTO_EN_PLLA=1, the DSPLL will automatically revert to the loop bandwidth when the loop has locked and LOL deasserts. See 1.4.1 Fastlock for more information on Fastlock behavior.

Table 14.132. Register 0x042C Holdover Exit Control for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x042C	0	R/W	HOLD_EN_PLLA	Holdover enable 0: Holdover Disabled 1: Holdover Enabled (default)
0x042C	3	R/W	HOLD_RAMP_BYP_PLLA	Must be set to 1 for Normal Operation.
0x042C	4	R/W	HOLD_EXITBW_SEL_PLLA	Selects the exit rate from Holdover bandwidth 0: Exit Holdover using Fastlock bandwidth (default) 1: Exit Holdover using the DSPLL loop bandwidth
0x042C	7:5	R/W	HOLD_RAMP_RATE_PLLA	Sets the base rate for ramped input switching and Holdover Entry/Exit. This value is multiplied by the RAMP_STEP_ADJ_PLLA factor to find the ramp rate. 0: 1.48 ppm/s 1: 2.22 ppm/s 2: 2.53 ppm/s 3: 1.18 ppm/s 4: 0.74 ppm/s 5: 5.06 ppm/s 6: 10.12 ppm/s 7: 40.48 ppm/s Ramp Rate = HOLD_RAMP_RATE_PLLA * RAMP_STEP_ADJ_PLLA

When a valid input is presented to the DSPLL while the device is in Holdover or Freerun mode, the higher Fastlock bandwidth can be enabled to provide faster DSPLL settling. When a slower response is desired, then the regular loop bandwidth may be used instead.

Table 14.133. Register 0x042E Holdover History Average Length for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x042E	4:0	R/W	HOLD_HIST_LEN_PLLA	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds: Window Length = $(2^{HOLD\_HIST\_LEN\_PLLA} - 1) \times 8 / 3 \times 10^{-7}$

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See 2.5 Holdover Mode to calculate the window length from the register value.

Table 14.134. Register 0x042F Holdover History Delay for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x042F	4:0	R/W	HOLD_HIST_DELAY_PLLA	Delay Time to ignore data at the end of the historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $2^{HOLD\_HIST\_DELAY\_PLLA} \times 2 / 3 \times 10^{-7}$

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See 2.5 Holdover Mode to calculate the ignore delay time from the register value.

Table 14.135. Register 0x0432-0x0424 Holdover Cycle Count DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0432	7:0	R/W	HOLD_15M_CYC_COUNT_PLLA	Value calculated in CBPro.
0x0433	15:8	R/W	HOLD_15M_CYC_COUNT_PLLA	
0x0434	23:16	R/W	HOLD_15M_CYC_COUNT_PLLA	

Table 14.136. Register 0x0435 Force Holdover for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0435	0	R/W	FORCE_HOLD_PLLA	Force the device into Holdover mode. Used to hold the device output clocks while retraining an upstream input clock. 0: Normal Operation 1: Force Holdover/Freerun Mode: HOLD_HIST_VALID_PLLA = 0 => Freerun Mode HOLD_HIST_VALID_PLLA = 1 => Holdover Mode

Table 14.137. Register 0x0436 Input Clock Switching Control for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0436	1:0	R/W	CLK_SWITCH_MODE_PLLA	Selects manual or automatic switching modes. Automatic mode can be Revertive or Non-revertive. 0: Manual (default) 1: Automatic Non-revertive 2: Automatic Revertive 3: Reserved
0x0436	2	R/W	HSW_EN_PLLA	Enable Hitless Switching. 0: Disable Hitless switching (default) 1: Enable Hitless switching (phase buildout enabled)

Table 14.138. Register 0x0437 Input Fault Masks for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0437	3:0	R/W	IN_LOS_MSK_PLLA	Enables the use of IN3 - IN0 LOS status in determining a valid clock for automatic input selection. 0: Use LOS in automatic clock switching logic (default) 1: Mask (ignore) LOS from automatic clock switching logic

Reg Address	Bit Field	Type	Name	Description
0x0437	7:4	R/W	IN_OOF_MSK_PLLA	Determines the OOF status for IN3 - IN0 and is used in determining a valid clock for the automatic input selection. 0: Use OOF in the automatic clock switching logic (default) 1: Mask (ignore) OOF from automatic clock switching logic

This register is for the input clock fault masks. For each of the four clock inputs, the OOF and/or the LOS fault can be used for the clock selection logic or they can be masked from it.

Note: The clock selection logic can affect entry into Holdover.

Table 14.139. Register 0x0438-0x0439 Clock Input Priorities for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0438	2:0	R/W	IN0_PRIORITY_PLLA	IN0 - IN3 priority assignment for the automatic switching state machine. Priority assignments in descending importance are: 1, 2, 3, 4 (or 0 for never select) 5-7: Reserved
0x0438	6:4	R/W	IN1_PRIORITY_PLLA	
0x0439	2:0	R/W	IN2_PRIORITY_PLLA	
0x0439	6:4	R/W	IN3_PRIORITY_PLLA	

This register is used to assign priority to each input clock for automatic clock input switching. The available clock with the highest priority will be selected. Priority 1 is first and most likely to be selected, followed by priorities 2-4. Priority 0 prevents the clock input from being automatically selected, though it may still be manually selected. When two valid input clocks are assigned the same priority, the lowest numbered input will be selected. In other words, IN0 has priority over IN1-IN3, IN1 has priority over IN2-IN3, etc, when the priorities are the same.

Table 14.140. Register 0x043A Hitless Switching Mode DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x043A	1:0	R/W	HSW_MODE_PLLA	1: Default setting, do not modify 0, 2, 3: Reserved
0x043A	3:2	R/W	HSW_PHMEAS_CTRL_PLLA	0: Default setting, do not modify 0, 2, 3: Reserved

Table 14.141. Register 0x043B–0x044C Hitless Switching Phase Threshold DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x043B	7:0	R/W	HSW_PHMEAS_THR_PLLA	Value calculated in CBPro.
0x043C	9:8	R/W	HSW_PHMEAS_THR_PLLA	

Table 14.142. Register 0x043D Hitless Switching Length DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x043D	4:0	R/W	HSW_COARSE_PM_LEN_PLLA	Value calculated in CBPro.

Table 14.143. Register 0x043E Hitless Switching Length DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x043E	4:0	R/W	HSW_COARSE_PM_DLY_PLLA	Value calculated in CBPro.

Table 14.144. Register 0x043F DSPLL Hold Valid and Fastlock Status for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x043F	1	R	HOLD_HIST_VALID_PLLA	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x043F	2	R	FASTLOCK_STATUS_PLLA	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLA accumulation will stop. When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 14.145. Register 0x0487 Zero Delay Mode Setup for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0487	0	R/W	ZDM_EN	Enable ZDM Operation. 0: Disable Zero Delay Mode (default) 1: Enable Zero Delay Mode
0x0487	2:1	R/W	ZDM_IN_SEL	ZDM Manual Input Source Select. 0: IN0 (default) 1: IN1 2: IN2 3: Reserved (IN3 already used by ZDM)

To enable ZDM, set ZDM_EN = 1. In ZDM, the input clock source must be selected manually by using either the ZDM_IN_SEL register bits or the IN_SEL1 and IN_SEL0 device input pins. IN_SEL_REGCTRL determiens the choice of register or pin control to select the desired input clock. When register control is selected in ZDM, the ZDM_IN_SEL control bits determine the input to be used and the non-ZDM IN_SEL bits will be ignored. Note that in ZDM, the DSPLL does not use either Hitless switching or Automatic input source switching.

Table 14.146. Register 0x0488 Fine Hitless Switching PM Length for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0488	3:0	R/W	HSW_FINE_PM_LEN_PLLA	Values set by CBPro.

Table 14.147. Register 0x0489 - 0x049A PFD Enable Delay for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x0489	7:0	R/W	PFD_EN_DE-LAY_PLLA	Set by CBPro.
0x048A	12:8	R/W	PFD_EN_DE-LAY_PLLA	

Table 14.148. Register 0x049B Holdover Exit for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x049B	1	R/W	INIT_LP_CLOSE_HO_PLLA	PLL acquisition method for Freerun to Lock transition. 0: Normal loop closure 1: Holdover exit ramp (default)
0x049B	4	R/W	HOLD_PRE-SERVE_HIST_PLLA	Preserve Holdover history when the input clock is lost or switched. 0: Clear Holdover history when the input clock is lost or switched. 1: Preserve Holdover history when the input clock is lost or switched. (default)
0x049B	5	R/W	HOLD_FRZ_WITH_INTON-LY_PLLA	Holdover Freeze control when the input clock is lost or switched. 0: Use filter output on Freeze. 1: Use Integrator-only on Freeze. (default)
0x049B	6	R/W	HOLDEXIT_BW_SEL0_PLLA	Set by CBPro.
0x049B	7	R/W	HOLDEXIT_STD_BO_PLLA	1: Default setting, do not modify 0: Reserved

Table 14.149. Register 0x049C Holdover Exit Control for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x049C	6	R/W	HOLDEX-IT_ST_BO_PLLA	Value set by CBPro.
0x049C	7	R/W	HOLD_RAMPBP_NO HIST_PLLA	Value set by CBPro.

Table 14.150. Register 0x049D-0x04A2 Holdover Exit Bandwidth for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x049D	7:0	R/W	HOLDEX-IT_BW0_PLLA	DSPLL A Holdover Exit bandwidth parameters calculated by CBPro when ramp switching is disabled.
0x049E	7:0	R/W	HOLDEX-IT_BW1_PLLA	
0x049F	7:0	R/W	HOLDEX-IT_BW2_PLLA	
0x04A0	7:0	R/W	HOLDEX-IT_BW3_PLLA	
0x04A1	7:0	R/W	HOLDEX-IT_BW4_PLLA	
0x04A2	7:0	R/W	HOLDEX-IT_BW5_PLLA	

This group of registers determines the DSPLL A bandwidth used when exiting Holdover Mode. In ClockBuilder Pro it is selectable from 200 Hz to 4 kHz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLA bit (reg 0x0414[0]) must be used to cause all of the BWx_PLLA, FAST_BWx_PLLA, and BWx_HO_PLLA parameters to take effect. Note that the individual SOFT_RST_PLLA (0x001C[1]) does not update these bandwidth parameters.

Table 14.151. Register 0x04A4 Hitless Switching Limit for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04A4	7:0	R/W	HSW_LIMIT_PLLA	Value set by CBPro.

Table 14.152. Register 0x04A5 Hitless Switching Limit Action for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04A5	0	R/W	HSW_LIMIT_ACTION_PLLA	Value set by CBPro.

Table 14.153. Register 0x04A6 Hitless Switching Ramp Control for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04A6	2:0	R/W	RAMP_STEP_ADJ_PLLA	Scaling factor for ramped input switching and Holdover Entry/Exit. Multiply with HOLD_RAMP_RATE_PLLA to calculate final ramp rate. 0: 1x 1: 4x 2: 16x 3: 64x 4: 256x 5: 1024x 6: 1/4x 7: 1/2x Ramp Rate = HOLD_RAMP_RATE_PLLA * RAMP_STEP_ADJ_PLLA
0x04A6	3	R/W	RAMP_SWITCH_EN_PLLA	Enable ramped input switching and entry into Holdover/Freerun. 0: Disable ramped input switching and entry into Holdover 1: Enable ramped input switching and entry into Holdover

Table 14.154. Register 0x04AC Configuration for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04AC	0	R/W	OUT_MAX_LIMIT_EN_PLLA	Set by CBPro.
0x04AC	3	R/W	HOLD_SETTLE_DET_EN_PLLA	Set by CBPro.

Table 14.155. Register 0x04AD - 0x04AE Configuration for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04AD	7:0	R/W	OUT_MAX_LIMIT_LMT_PLLA	Set by CBPro.
0x04AE	15:0	R/W		

Table 14.156. Register 0x04B1 - 0x04B2 Configuration for DSPLL A

Reg Address	Bit Field	Type	Name	Description
0x04B1	7:0	R/W	HOLD_SETTLE_TARGET_PLLA	Set by CBPro.
0x04B2	15:0	R/W		

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Table 14.157. Register 0x0507 Input Selection for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0507	7:6	R	IN_ACTV_PLLB	Currently selected DSPLL B input clock. 0: IN0 1: IN1 2: IN2 3: IN3

This register displays the currently selected input for the DSPLL. In manual select mode, this reflects either the register value or the voltages on the IN_SEL1 and IN_SEL0 pins. In automatic switching mode, it reflects the input currently chosen by the automatic algorithm. If there are no valid input clocks in the automatic mode, this value will retain its previous value until a valid input clock is presented. Note that this value is not meaningful in Holdover or Freerun modes.

Table 14.158. Register 0x0508-0x050D DSPLL Loop Bandwidth for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0508	7:0	R/W	BW0_PLLB	DSPLL B loop bandwidth parameters.
0x0509	7:0	R/W	BW1_PLLB	
0x050A	7:0	R/W	BW2_PLLB	
0x050B	7:0	R/W	BW3_PLLB	
0x050C	7:0	R/W	BW4_PLLB	
0x050D	7:0	R/W	BW5_PLLB	

This group of registers determines the DSPLL B loop bandwidth. In ClockBuilder Pro it is selectable from 10 Hz to 100 Hz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 14.159. Register 0x050E-0x0513 DSPLL Fastlock Loop Bandwidth for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x050E	7:0	R/W	FAST_BW0_PLLB	DSPLL B Fastlock Bandwidth parameters.
0x050F	7:0	R/W	FAST_BW1_PLLB	
0x0510	7:0	R/W	FAST_BW2_PLLB	
0x0511	7:0	R/W	FAST_BW3_PLLB	
0x0512	7:0	R/W	FAST_BW4_PLLB	
0x0513	7:0	R/W	FAST_BW5_PLLB	

This group of registers determines the DSPLL Fastlock bandwidth. In ClockBuilder Pro, it is selectable from 10 Hz to 4 kHz in factors of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that individual SOFT_RST_PLLB (0x001C[2]) does not update the bandwidth parameters.

Table 14.160. Register 0x0514 DSPLL Bandwidth Update for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0514	0	S	BW_UPDATE_PLLB	Set to 1 to latch updated BWx_PLLB and FAST_BWx_PLLB bandwidth registers into operation.

Setting this self-clearing bit high latches all of the new DSPLL B bandwidth register values into operation. Asserting this strobe will update all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB bandwidths at the same time. A device Soft Reset (0x001C[0]) will have the same effect, but individual DSPLL soft resets will not update these values.

Table 14.161. Register 0x0515-0x051B M Feedback Divider Numerator, 56-bits for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0515	7:0	R/W	M_NUM_PLLB	M feedback divider Numerator 56-bit Integer
0x0516	15:8			
0x0517	23:16			
0x0518	31:24			
0x0519	39:32			
0x051A	47:40			
0x051B	55:48			

Note that DSPLL B includes a divide-by-5 block in the PLL feedback path before the M divider. Register values for the DSPLL B M divider must account for this additional divider. This divider is not present in DSPLLs A, C, or D.

Table 14.162. Register 0x051C-0x051F M Feedback Divider Denominator, 32-bits for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x051C	7:0	R/W	M_DEN_PLLB	M feedback divider Denominator 32-bit Integer
0x051D	15:8			
0x051E	23:16			
0x051F	31:24			

The DSPLL M feedback divider values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers. An Integer ratio of (M_NUM / M_DEN) will give the best phase noise performance.

Note: There is a divide-by-5 prescaler before the DSPLL B M divider, so if (M_NUM / M_DEN) = 100, the effective feedback divide ratio (Fvco / Fpfd) will be 500.

Table 14.163. Register 0x0520 M Divider Update for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0520	0	S	M_UPDATE_PLLB	Set this bit to latch the M feedback divider register values into operation.

Setting this self-clearing bit high latches the new M feedback divider register values into operation. A Soft Reset will have the same effect.

Table 14.164. Register 0x0521 M Divider Fractional Enable for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0521	3:0	R/W	M_FRAC_MODE_PLLB	M feedback divider fractional mode. Must be set to 0xB for proper operation
0x0521	4	R/W	M_FRAC_EN_PLLB	M feedback divider fractional enable. 0: Integer-only division 1: Fractional (or integer) division - Required for DCO operation.
0x0521	5	R/W	Reserved	Must be set to 0 for DSPLL B

Table 14.165. Register 0x052A Input Clock Select for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x052A	0	R/W	IN_SEL_REGCTRL_PLLB	Manual Input Select control source. 0: Pin controlled input clock selection (default) 1: IN_SEL register input clock selection (ZDM_IN_SEL in ZDM)
0x052A	3:1	R/W	IN_SEL_PLLB	Manual Input Select selection register. (Non-ZDM) 0: IN0 (default), 1: IN1, 2: IN2, 3: IN3, 4-7: Reserved

Input clock selection for manual register based and pin controlled clock selection. Note that in ZDM, the ZDM_IN_SEL (0x0487[2:1]) input source select control bits are used and IN_SEL is ignored. In both ZDM and non-ZDM operation, IN_SEL_REGCTRL determines whether register-based or pin-based manual source selection is used.

Note: When IN_SEL_REGCTRL is low, IN_SEL does not do anything and the clock selection is pin controlled.

Table 14.166. Register 0x052B Fastlock Control for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN_PLLB	Auto Fastlock Enable/Disable. 0: Disable Auto Fastlock (default) 1: Enable Auto Fastlock
0x052B	1	R/W	FASTLOCK_MAN_PLLB	Manually Force Fastlock. 0: Normal Operation (default) 1: Force Fastlock

When Fastlock is enabled by either manual or automatic means, the higher Fastlock bandwidth will be used to provide faster settling of the DSPLL. With FASTLOCK_MAN_PLLB=0 and FASTLOCK_AUTO_EN_PLLB=1, the DSPLL will automatically revert to the loop bandwidth when the loop has locked and LOL deasserts. See 1.4.1 Fastlock for more information on Fastlock behavior.

Table 14.167. Register 0x052C Holdover Exit Control for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x052C	0	R/W	HOLD_EN_PLLB	Holdover enable 0: Holdover Disabled 1: Holdover Enabled (default)
0x052C	3	R/W	HOLD_RAMP_BYP_PLLB	Must be set to 1 for Normal Operation.
0x052C	4	R/W	HOLD_EXIT_BW_SEL_PLLB	Selects the exit from Holdover bandwidth when ramped exit is disabled by the user. 0: Exit Holdover using Fastlock bandwidth (default) 1: Exit Holdover using the DSPLL loop bandwidth
0x052C	7:5	R/W	HOLD_RAMP_RATE_PLLB	Sets the base rate for ramped input switching and Holdover Entry/Exit. This value is multiplied by the RAMP_STEP_ADJ_PLLB factor to find the ramp rate. 0: 1.48ppm/s 1: 2.22ppm/s 2: 2.53ppm/s 3: 1.18ppm/s 4: 0.74 ppm/s 5: 5.06 ppm/s 6: 10.12 ppm/s 7: 40.48 ppm/s Ramp Rate = HOLD_RAMP_RATE_PLLB * RAMP_STEP_ADJ_PLLB

When a valid input is presented to the DSPLL while the device is in Holdover or Freerun mode, the higher Fastlock bandwidth can be enabled to provide faster DSPLL settling. When a slower response is desired, then the regular loop bandwidth may be used instead.

Table 14.168. Register 0x052E Holdover History Average Length for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN_PLLB	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds: Window Length = $(2^{HOLD\_HIST\_LEN\_PLLB} - 1) \times 8 / 3 \times 10^{-7}$

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See 2.5 Holdover Mode to calculate the window length from the register value.

Table 14.169. Register 0x052F Holdover History Delay for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x052F	4:0	R/W	HOLD_HIST_DELAY_PLLB	Delay Time to ignore data at the end of the historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $2^{HOLD\_HIST\_DELAY\_PLLB} \times 2 / 3 \times 10^{-7}$

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See 2.5 Holdover Mode to calculate the ignore delay time from the register value.

Table 14.170. Register 0x05320x0524 Holdover Cycle Count DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0532	7:0	R/W	HOLD_15M_CYC_COUNT_PLLB	Value calculated in CBPro.
0x0533	15:8	R/W	HOLD_15M_CYC_COUNT_PLLB	
0x0534	23:16	R/W	HOLD_15M_CYC_COUNT_PLLB	

Table 14.171. Register 0x0535 Force Holdover for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0535	0	R/W	FORCE_HOLD_PLLB	Force the device into Holdover mode. Used to hold the device output clocks while retraining an upstream input clock. 0: Normal Operation 1: Force Holdover/Freerun Mode: HOLD_HIST_VALID_PLLB = 0 => Freerun Mode HOLD_HIST_VALID_PLLB = 1 => Holdover Mode

Table 14.172. Register 0x0536 Input Clock Switching Control for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0536	1:0	R/W	CLK_SWITCH_MODE_PLLB	Selects manual or automatic switching modes. Automatic mode can be Revertive or Non-revertive. 0: Manual (default) 1: Automatic Non-revertive 2: Automatic Revertive 3: Reserved

Reg Address	Bit Field	Type	Name	Description
0x0536	2	R/W	HSW_EN_PLLB	Enable Hitless Switching. 0: Disable Hitless switching (default) 1: Enable Hitless switching (phase buildout enabled)

Table 14.173. Register 0x0537 Input Fault Masks for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0537	3:0	R/W	IN_LOS_MSK_PLLB	Enables the use of IN3 - IN0 LOS status in determining a valid clock for automatic input selection. 0: Use LOS in automatic clock switching logic (default) 1: Mask (ignore) LOS from automatic clock switching logic
0x0537	7:4	R/W	IN_OOF_MSK_PLLB	Determines the OOF status for IN3 - IN0 and is used in determining a valid clock for the automatic input selection. 0: Use OOF in the automatic clock switching logic (default) 1: Mask (ignore) OOF from automatic clock switching logic

This register is for the input clock fault masks. For each of the four clock inputs, the OOF and/or the LOS fault can be used for the clock selection logic or they can be masked from it.

Note: The clock selection logic can affect entry into Holdover.

Table 14.174. Register 0x0538-0x0539 Clock Input Priorities for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0538	2:0	R/W	IN0_PRIORITY_PLLB	IN0 - IN3 priority assignment for the automatic switching state machine. Priority assignments in descending importance are: 1, 2, 3, 4 (or 0 for no priority) 5-7: Reserved
0x0538	6:4	R/W	IN1_PRIORITY_PLLB	
0x0539	2:0	R/W	IN2_PRIORITY_PLLB	
0x0539	6:4	R/W	IN3_PRIORITY_PLLB	

This register is used to assign priority to each input clock for automatic clock input switching. The available clock with the highest priority will be selected. Priority 1 is first and most likely to be selected, followed by priorities 2-4. Priority 0 prevents the clock input from being automatically selected, though it may still be manually selected. When two valid input clocks are assigned the same priority, the lowest numbered input will be selected. In other words, IN0 has priority over IN1-IN3, IN1 has priority over IN2-IN3, etc, when the priorities are the same.

Table 14.175. Register 0x053A Hitless Switching Mode DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x053A	1:0	R/W	HSW_MODE_PLLB	1: Default setting, do not modify 0, 2, 3: Reserved
0x053A	3:2	R/W	HSW_PHMEAS_CTRL_PLLB	0: Default setting, do not modify 1, 2, 3: Reserved

Table 14.176. Register 0x053B–0x053C Hitless Switching Phase Threshold DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x053B	7:0	R/W	HSW_PHMEAS_THR_PLLB	Value calculated in CBPro.
0x053C	9:8	R/W	HSW_PHMEAS_THR_PLLB	

Table 14.177. Register 0x053D Hitless Switching Length DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x053D	4:0	R/W	HSW_COARSE_PM_LEN_PLLB	Value calculated in CBPro.

Table 14.178. Register 0x053E Hitless Switching Length DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x053E	4:0	R/W	HSW_COARSE_PM_DLY_PLLB	Value calculated in CBPro.

Table 14.179. Register 0x053F DSPLL Hold Valid and Fastlock Status for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x053F	1	R	HOLD_HIST_VALID_PLLB	Holdover Valid historical frequency data indicator. 0: Invalid Holdover History - Freerun on input fail or switch 1: Valid Holdover History - Holdover on input fail or switch
0x053F	2	R	FASTLOCK_STATUS_PLLB	Fastlock engaged indicator. 0: DSPLL Loop BW is active 1: Fastlock DSPLL BW currently being used

When the input fails or is switched and the DSPLL switches to Holdover or Freerun mode, HOLD_HIST_VALID_PLLB accumulation will stop. When a valid input clock is presented to the DSPLL, the holdover frequency history measurements will be cleared and will begin to accumulate once again.

Table 14.180. Register 0x0540 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0540	7:0	R/W	RESERVED	Reserved.

This register is used when making certain changes to the device. See Section 2.1.1 Updating Registers During Device Operation for more information.

Table 14.181. Register 0x0588 Fine Hitless Switching PM Length for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0588	3:0	R/W	HSW_FINE_PM_LEN_PLLB	Values set by CBPro.

Table 14.182. Register 0x0589 - 0x059A PFD Enable Delay for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x0589	7:0	R/W	PFD_EN_DELAY_PLLB	Set by CBPro.
0x058A	12:8	R/W	PFD_EN_DELAY_PLLB	

Table 14.183. Register 0x059B Holdover Exit for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x059B	1	R/W	INIT_LP_CLOSE_HO_PLLB	PLL acquisition method for Freerun to Lock transition. 0: Normal loop closure 1: Holdover exit ramp (default)
0x059B	4	R/W	HOLD_PRESERVE_HIST_PLLB	Preserve Holdover history when the input clock is lost or switched. 0: Clear Holdover history when the input clock is lost or switched. 1: Preserve Holdover history when the input clock is lost or switched. (default)
0x059B	5	R/W	HOLD_FRZ_WITH_INTONLY_PLLB	Holdover Freeze control when the input clock is lost or switched. 0: Use filter output on Freeze. 1: Use Integrator-only on Freeze. (default)
0x059B	6	R/W	HOLDEXIT_BW_SEL0_PLLB	Set by CBPro.
0x059B	7	R/W	HOLDEXIT_STD_BO_PLLB	1: Default setting, do not modify 0: Reserved

Table 14.184. Register 0x059C Holdover Exit Control for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x059C	6	R/W	HOLDEX-IT_ST_BO_PLLB	Value set by CBPro.
0x059C	7	R/W	HOLD_RAMPBP_NO HIST_PLLB	Value set by CBPro.

Table 14.185. Register 0x059D-0x05A2 Holdover Exit Bandwidth for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x059D	7:0	R/W	HOLDEX-IT_BW0_PLLB	DSPLL B Holdover Exit bandwidth parameters calculated by CBPro when ramp switching is disabled.
0x059E	7:0	R/W	HOLDEX-IT_BW1_PLLB	
0x059F	7:0	R/W	HOLDEX-IT_BW2_PLLB	
0x05A0	7:0	R/W	HOLDEX-IT_BW3_PLLB	
0x05A1	7:0	R/W	HOLDEX-IT_BW4_PLLB	
0x05A2	7:0	R/W	HOLDEX-IT_BW5_PLLB	

This group of registers determines the DSPLL B bandwidth used when exiting Holdover Mode. In ClockBuilder Pro it is selectable from 10 Hz to 100 Hz in steps of roughly 2x each. ClockBuilder Pro will then determine the values for each of these registers. Either a full device SOFT_RST_ALL (0x001C[0]) or the BW_UPDATE_PLLB bit (reg 0x0514[0]) must be used to cause all of the BWx_PLLB, FAST_BWx_PLLB, and BWx_HO_PLLB parameters to take effect. Note that the individual SOFT_RST_PLLB (0x001C[2]) does not update these bandwidth parameters.

Table 14.186. Register 0x05A4 Hitless Switching Limit for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05A4	7:0	R/W	HSW_LIMIT_PLLB	Value set by CBPro.

Table 14.187. Register 0x05A5 Hitless Switching Limit Action for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05A5	0	R/W	HSW_LIMIT_AC-TION_PLLB	Value set by CBPro.

Table 14.188. Register 0x05A6 Hitless Switching Ramp Control for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05A6	2:0	R/W	RAMP_STEP_ADJ_PLLB	Scaling factor for ramped input switching and Holdover Entry/Exit. Multiply with HOLD_RAMP_RATE_PLLB to calculate final ramp rate. 0: 1x 1: 4x 2: 16x 3: 64x 4: 256x 5: 1024x 6: 1/4x 7: 1/2x Ramp Rate = HOLD_RAMP_RATE_PLLB * RAMP_STEP_ADJ_PLLB
0x05A6	3	R/W	RAMP_SWITCH_EN_PLLB	Enable ramped input switching and entry into Holdover/Freerun. 0: Disable ramped input switching and entry into Holdover 1: Enable ramped input switching and entry into Holdover

Table 14.189. Register 0x05AC Configuration for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05AC	0	R/W	OUT_MAX_LIMIT_EN_PLLB	Set by CBPro.
0x05AC	3	R/W	HOLD_SETTLE_DET_EN_PLLB	Set by CBPro.

Table 14.190. Register 0x05AD - 0x05AE Configuration for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05AD	7:0	R/W	OUT_MAX_LIMIT_LMT_PLLB	Set by CBPro.
0x05AE	15:0	R/W		

Table 14.191. Register 0x05B1 - 0x05B2 Configuration for DSPLL B

Reg Address	Bit Field	Type	Name	Description
0x05B1	7:0	R/W	HOLD_SETTLE_TARGET_PLLB	Set by CBPro.
0x05B2	15:0	R/W		

14.7 Page 9 Registers

Table 14.192. Register 0x090E External XAXB Source Select

Reg Address	Bit Field	Type	Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	Must always be set to '1' for external XO operation on XA/XB.

Table 14.193. Register 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Name	Description
0x0943	0	R/W	IO_VDD_SEL	Select digital I/O operating voltage. 0: 1.8 V digital I/O connections 1: 3.3 V digital I/O connections

The IO_VDD_SEL configuration bit selects between 1.8 V and 3.3 V digital I/O. All digital I/O pins, including the serial interface pins, are 3.3 V tolerant with either setting. The default 1.8 V setting (0x0943 = 0x0) is the safe default choice that allows writes to the device regardless of the serial interface used or the host supply voltage. When the I^2C or SPI host is operating at 3.3 V and the Si5381/82 at VDD=1.8 V, the host must write IO_VDD_SEL=1 first. This will ensure that both the host and the serial interface are operating with the optimum signal thresholds.

Table 14.194. Register 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0949	3:0	R/W	IN_EN	Enable (or powerdown) the IN3 - IN0 input buffers. 0: Powerdown input buffer 1: Enable and Power-up input buffer
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	Select Pulsed CMOS input buffer for IN3-IN0. See 3.2 Types of Inputs for more information. 0: Standard Input Format 1: Pulsed CMOS Input Format

When a clock input is disabled, it is powered down as well.

- IN0: IN_EN 0x0949[0], IN_PULSED_CMOS_EN 0x0949[4]
- IN1: IN_EN 0x0949[1], IN_PULSED_CMOS_EN 0x0949[5]
- IN2: IN_EN 0x0949[2], IN_PULSED_CMOS_EN 0x0949[6]
- IN3: IN_EN 0x0949[3], IN_PULSED_CMOS_EN 0x0949[7]

Table 14.195. Register 0x094A Input Clock Enable to DSPLL

Reg Address	Bit Field	Type	Name	Description
0x094A	3:0	R/W	INX_TO_PFD_EN	Value calculated in CBPro.

Table 14.196. Register 0x094E–0x094F Input Clock Buffer Hysteresis

Reg Address	Bit Field	Type	Name	Description
0x094E	7:0	R/W	REFCLK_HYS_SEL	Value calculated in CBPro.
0x094F	3:0	R/W	REFCLK_HYS_SEL	

Table 14.197. Register 0x094F Input CMOS Threshold Select

Reg Address	Bit Field	Type	Name	Description
0x094F	7:4	R/W	CMOS_HI_THR	CMOS Clock input threshold select for inputs IN3-IN0. 0: Low threshold (Pulsed CMOS) 1: Standard Threshold - Use with DC coupled CMOS input clocks

14.8 Page A Registers

Table 14.198. Register 0x0A02 Enable N-divider 0.5x

Reg Address	Bit Field	Type	Name	Description
0x0A02	4:0	R/W	N_ADD_0P5	Value calculated in CBPro.

Table 14.199. Register 0x0A03 Output N Divider to Output Driver

Reg Address	Bit Field	Type	Name	Description
0x0A03	4:0	R/W	N_CLK_TO_OUTX_EN	Enable output clocks from N[4:0]. 0: N divider output disabled. 1: N divider output enabled.

Note: In the Si5382, N0 MUST be enabled when DSPLL A is active. ClockBuilder Pro determines these values when changing settings for the device.

Table 14.200. Register 0x0A04 Output N Divider Integer Divide Mode

Reg Address	Bit Field	Type	Name	Description
0x0A04	4:0	R/W	N_PIBYP	Bypass fractional divider for N[4:0]. 0: Fractional (or Integer) division - Required for N0. Optional for N1-N4. Recommended when changing settings during operation 1: Integer-only division - best phase noise - Recommended for Si5382 N1-N4 when Integer Note that a device Soft Reset (0x001C[0]=1) must be issued after changing the settings in this register.

Note: In the Si5382, must be set to 0x0 for N0 when DSPLL A is active. Provides a small improvement in phase noise when used with integer N1- N4. ClockBuilder Pro determines these values when changing settings for the device.

Table 14.201. Register 0x0A05 Output N Divider Power Down

Reg Address	Bit Field	Type	Name	Description
0x0A05	4:0	R/W	N_PDNB	Powerdown unused N dividers N[4:0] 0: N divider powered down 1: N divider powered up and enabled

Note: N0 (DSPLL A) MUST be enabled when DSPLLA is active. ClockBuilder Pro determines these values when changing settings for the device.

Table 14.202. Register 0x0A14 Output N0 Divider Auto-Disable

Reg Address	Bit Field	Type	Name	Description
0x0A14	3	R/W	N0_LOAD_AUTO_DIS	Set by CBPro.

Table 14.203. Register 0x0A1A Output N1 Divider Auto-Disable

Reg Address	Bit Field	Type	Name	Description
0x0A1A	3	R/W	N1_LOAD_AUTO_DIS	Set by CBPro.

Table 14.204. Register 0x0A20 Output N2 Divider Auto-Disable

Reg Address	Bit Field	Type	Name	Description
0x0A20	3	R/W	N2_LOAD_AUTO_DIS	Set by CBPro.

Table 14.205. Register 0x0A26 Output N3 Divider Auto-Disable

Reg Address	Bit Field	Type	Name	Description
0x0A26	3	R/W	N3_LOAD_AUTO_DIS	Set by CBPro.

Table 14.206. Register 0x0A2C Output N4 Divider Auto-Disable

Reg Address	Bit Field	Type	Name	Description
0x0A2C	3	R/W	N4_LOAD_AUTO_DIS	Set by CBPro.

14.9 Page B Registers

Table 14.207. Register 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See 2.1.1 Updating Registers During Device Operation for more information.

Table 14.208. Register 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See 2.1.1 Updating Registers During Device Operation for more information.

Table 14.209. Register 0x0B44 Clock Control for Fractional Dividers

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Clock Disable for the fractional divide of the input P dividers. [P3, P2, P1, P0]. Must be set to a 0 if the P divider has a fractional value. 0: Enable the clock to the fractional divide part of the P divider. 1: Disable the clock to the fractional divide part of the P divider.
0x0B44	4	R/W	FRACN_CLK_DIS_PLLA	Clock disable for the fractional divide of the M divider in PLLA. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	5	R/W	FRACN_CLK_DIS_PLLB	Clock disable for the fractional divide of the M divider in PLLB. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Table 14.210. Register 0x0B45 LOL Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B45	0	R/W	CLK_DIS_PLLA	Disable PLL A LOL clock. Must be 0 for normal LOL operation.

Reg Address	Bit Field	Type	Name	Description
0x0B45	1	R/W	CLK_DIS_PLLB	Disable PLL B LOL clock. Must be 0 for normal LOL operation.

Table 14.211. Register 0x0B46 Loss of Signal Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Disables LOS clock for IN3 - IN0. Must be set to 0 to enable the LOS function of the respective inputs.

ClockBuilder Pro handles these bits when changing settings for all portions of the device.

Table 14.212. Register 0x0B47 DSPLL OOF Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B47	4, 1:0	R/W	OOF_CLK_DIS	Bits 1:0 disable OOF clocks for DSPLLs B:A. Bit 4 disables the OOF clock for the XAXB reference clock. Set to 0 for normal operation.

Table 14.213. Register 0x0B48 DSPLL OOF Divider Disables

Reg Address	Bit Field	Type	Name	Description
0x0B48	4, 1:0	R/W	OOF_DIV_CLK_DIS	Bits 1:0 disable OOF divider for DSPLLs B:A. Bit 4 disables the OOF clock for the XAXB reference clock. Set to 0 for normal operation.

Table 14.214. Register 0x0B49 Reserved Control_2

Reg Address	Bit Field	Type	Name	Description
0x0B49	1:0	R/W	CAL_DIS	Must be 0 for normal operation.
0x0B49	3:2	R/W	CAL_FORCE	Must be 0 for normal operation.

ClockBuilder Pro handles these bits when changing settings for the device.

Table 14.215. Register 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	4:0	R/W	N_CLK_DIS	Disable digital clocks from each DSPLL [1 D C B A] to the N dividers. The most significant bit must always be set to 1. Bits 3:0 must be set to 0 to use the corresponding DSPLL output. See also related registers 0x0A03 and 0x0A05.
0x0B4A	5	R/W	M_CLK_DIS	Disable M divider. Must be set to 0 to enable the M divider.
0x0B4A	6	R/W	M_DIV_CAL_DIS	Disable M divider calibration. Must be set to 0 to allow calibration.

ClockBuilder Pro handles these bits when changing settings for the device.

Table 14.216. Register 0x0B57-0B58 VCO Calcode

Reg Address	Bit Field	Type	Name	Description
0x0B57	7:0	R/W	VCO_RESET_CAL-CODE	Value calculated in CBPro.
0x0B58	3:0	R/W	VCO_RESET_CAL-CODE	

14.10 Page C Registers

Table 14.217. Register 0x0C02 Clock Validation Configuration

Reg Address	Bit Field	Type	Name	Description
0x0C02	2:0	R/W	VAL_DIV_CTL0	Set by CBPro.
0x0C02	4	R/W	VAL_DIV_CTL1	Set by CBPro.

Table 14.218. Register 0x0C03 Clock Validation Configuration

Reg Address	Bit Field	Type	Name	Description
0x0C03	3:0	R/W	IN_CLK_VAL_PWR_UP_DIS	Set by CBPro.

Table 14.219. Register 0x0C07 Clock Validation Configuration

Reg Address	Bit Field	Type	Name	Description
0x0C07	0	R/W	IN_CLK_VAL_EN	Set by CBPro.

Table 14.220. Register 0x0C08 Clock Validation Configuration

Reg Address	Bit Field	Type	Name	Description
0x0C08	7:0	R/W	IN_CLK_VAL_TIME	Set by CBPro.

15. Appendix—Custom Differential Amplitude Controls

In some customer applications, it may be desirable to have larger or smaller differential amplitudes than those produced by the standard LVPECL and LVDS settings generated by ClockBuilder Pro. For example, "CML" format is sometimes desired for an application, but CML is not a defined standard, and, hence, the input amplitude of CML signals may differ between receivers. In these cases, the following information describes how to implement nonstandard differential amplitudes.

The differential output driver has two basic modes of operation as well as variable output amplitude capability. The Normal mode has an internal impedance of 100 Ω differential, while the Low Power mode has an internal impedance of >500 Ω differential. In both cases, when properly terminated with 100 Ω differential externally, the typical amplitudes listed in the table below result.

Table 15.1. Differential Output Amplitude Typical Values

OUTx_AMPL	Normal Mode OUTx_FORMAT = 1 (mVpp-SE)	Low-Power Mode OUTx_FORMAT = 2 (mVpp-SE)
0	130	200
1	230	400
2	350	620
3	450	820
4	575	1010
5	700	1200
6	810	1350[1]
7	920	1600[1]

Note:
1. In Low-Power mode with VDDO=1.8 V, OUTx_AMPL may not be set to 6 or 7.
2. These amplitudes are based upon 100 Ω differential termination.

For applications using a custom differential output amplitude, the common mode voltage should be selected as shown in the table below. These selections, along with the settings given in Table 4.7 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML on page 45, have been verified to produce good signal integrity. Some extreme combinations of amplitude and common mode may have impaired signal integrity.

Also, in cases where the receiver is dc-based, either internally or through an external network, the outputs of the device must be ac-coupled. Output driver performance is not guaranteed when dc-coupled to a biased-input receiver.

Table 15.2. Differential Output Common Mode Voltage Selections

VDDO (Volts)	Differential Format	OUTx_FORMAT	Common Mode Voltage (Volts)	OUTx_CM
3.3	Normal	0x1	2.0	0xB
3.3	Low-Power	0x2	1.6	0x7
2.5	Normal	0x1	1.3	0xC
2.5	Low-Power	0x2	1.1	0xA
1.8	Normal	0x1	0.8	0xD
1.8	Low-Power	0x2	0.8	0xD

See also Table 4.7 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML on page 45 for additional information on the OUTx_FORMAT_OUTx_AMPL, and OUTx_CM controls.

16. Revision History

Revision 0.5

November 20, 2017

- Updated 2.1.2 NVM Programming.

Revision 0.4

September 21, 2017

- Initial release.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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