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August 2006

FMS6406
Precision S-Video Filter with Summed Composite Output, Sound Trap, and Group Delay Compensation

Features

- 7.6MHz 5th-order Y,C filters with composite summer
- 14dB notch at 4.425MHz to 4.6MHz for sound trap capable of handling stereo
- 50dB stopband attenuation at 27MHz on Y, C, and CV outputs
- Better than 0.5dB flatness to 4.2MHz on Y, C, and CV outputs
- Equalizer and notch filter for driving RF modulator with group delay of -180ns
- No external frequency selection components or clocks
- < 5ns group delay on Y, C, and CV outputs
- AC coupled inputs
- AC or DC coupled outputs
- Capable of PAL frequency for Y, C, CV
- Continuous Time Low Pass Filters
- <1.4% differential gain with 0.7° differential phase on Y, C, and CV channels
- Integrated DC restore circuitry with low tilt

Applications

- Cable set-top boxes
- Satellite set-top boxes
- DVD players

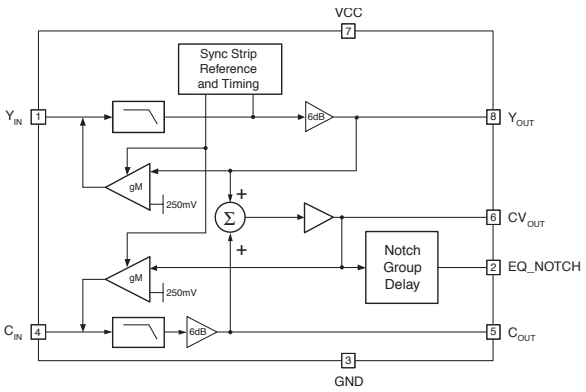
Description

The FMS6406 is a dual Y/C 5th-order Butterworth lowpass video filter optimized for minimum overshoot and flat group delay. The device also contains a summing circuit to generate filtered composite video, an audio trap and group delay compensation circuit. The audio trap removes video information in the spectral location of the subsequent RF audio carrier. The group delay circuit predistorts the signal to compensate for the inherent receiver IF filter's group delay distortion.

In a typical application, the Y and C input signals from DACs are AC-coupled into the filters. Both channels have DC-restore circuitry to clamp the DC-input levels during video sync. The Y and C channels use separate feedback clamps. The clamp pulse is derived from the Y channel.

All outputs are capable of driving $2V_{pp}$, AC or DC-coupled, into either a single or dual video load. A single video load consists of a series 75Ω impedance matching resistor connected to a terminated 75Ω line, this presents a total of 150Ω of loading to the part. A dual load would be two of these in parallel which would present a total of 75Ω to the part. The gain of the Y, C and CV signals is 6dB with $1V_{pp}$ input levels. All video channels are clamped during sync to establish the appropriate output voltage reference levels.

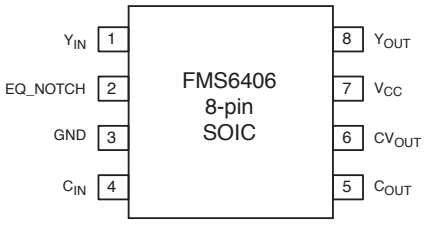
Block Diagram



Ordering Information

Part Number	Package	Pb-Free	Operating Temp Range	Packaging Method
FMS6406CS	SOIC-8	Yes	0°C to +70°C	Tube
FMS6406CSX	SOIC-8	Yes	0°C to +70°C	Tape and Reel

FMS6406 Pin Configuration



Pin Assignments

Pin#	Pin	Type	Description
1	Y_{IN}	Input	Luminance (Luma) Input: In a typical system, this pin is connected to the Luma or composite video output pin from the external video encoder.
2	EQ_NOTCH	Output	Composite video output to RF modulator/driver.
3	GND	Input	Ground
4	C_{IN}	Input	Chrominance (Chroma) Input: In a typical system, this pin is connected to the Chroma output pin from the external video encoder.
5	C_{OUT}	Output	Filtered Chrominance Video Output from the C_{IN} channel.
6	CV_{OUT}	Output	Composite Video Output: This pin is the sum of Y_{OUT} and C_{OUT}.
7	V_{CC}	Input	+5V supply.
8	Y_{OUT}	Output	Filtered Luminance Video Output from the Y_{IN} channel.

Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table defines the conditions for actual device operation.

Parameter	Min.	Max.	Unit
V_{CC}	-0.3	6	V
Analog and Digital I/O	-0.3	V_{CC} + 0.3	V
Output Channel - Any One Channel (Do Not Exceed)		100	mA

Notes:
Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if operating conditions are not exceeded.

Reliability Information

Parameter	Min.	Typ.	Max.	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		+150	°C
Lead Temperature (Soldering, 10s)			300	°C
Thermal Resistance (θ_{JA}), JEDEC Standard Multi-layer Test Boards, Still Air		115		°C/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	0		70	°C
V_{CC} Range	+4.75	+5.0	+5.25	V
GND		0		V

Electrical Characteristics

T_c = 25°C, V_i = 1V_{pp}, V_{CC} = 5V, all inputs AC-coupled with 0.1µF, all outputs are AC-coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current[1]	V_{CC} no load	50	80	110	mA
AV_{YCCV}	Low Frequency Gain (Y_{OUT}, C_{OUT}, CV_{OUT})[1]	at 400kHz	5.8	6.0	6.2	dB
AV_{EQ}	Low Frequency Gain (EQ_NOTCH)[1]	at 400kHz	5.7	6.0	6.4	dB
C_{sync}	C_{OUT} Output Level (during Sync)[1]	Sync present on Y_{IN} (after 6dB gain)	1.0	1.1	1.3	V
Y_{sync}	Y_{OUT} Output Level (during Sync)[1]	Sync present on Y_{IN} (after 6dB gain)		0.35	0.5	V
CV_{sync}	CV_{OUT} Output Level (during Sync)[1]	Sync present on Y_{IN} (after 6dB gain)		0.35	0.5	V
EQ_{sync}	EQ_NOTCH Output Level (during Sync)[1]	Sync present on Y_{IN} (after 6dB gain)		0.35	0.5	V
T_{CLAMP}	Clamp Response Time (Y Channel)	Settled to within 10mV		5		ms
f_{FLAT}	Gain Flatness to 4.2MHz[2] (Y_{OUT}, C_{OUT}, CV_{OUT})		-0.5	0	0.5	dB
f_C	-3dB Bandwidth[1]	Y, C, CV Channels	6.7	7.6		MHz
f_{SB}	Stopband Attenuation[1] (Y_{OUT}, C_{OUT}, CV_{OUT})	at 27MHz	40	50		dB
V_i	Input Signal Dynamic Range	All Channels/AC coupled		1.4		V_{pp}
I_{SC}	Output Short Circuit Current[4] (Any One Channel)	Y, C, CV, EQ_NOTCH to GND		85		mA
dG	Differential Gain[2]	Y, C, CV		1.4	3	%
dθ	Differential Phase[2]	Y, C, CV		0.7	1.5	°
THD	Output Distortion (All Channels)	V_{OUT} = 1.8V_{pp} at 3.58MHz		0.3		%
X_{TALK}	Crosstalk (Channel-to-Channel)	at 3.58MHz		-50		dB
PSRR	PSRR (All Channels)	DC		50		dB
SNR	SNR Y, C Channel[2]	NTC-7 weighting 4.2MHz lowpass	70	75		dB
	SNR CV Channel[2]	NTC-7 weighting 4.2MHz lowpass	70	75		dB
	SNR EQ_NOTCH Channel[2]	NTC-7 weighting 4.2MHz lowpass	65	70		dB
t_{pd}	Propagation Delay (Y, C, CV)	at 400kHz		112		ns
GD	Group Delay (Y, C, CV)[2]	at 3.58MHz (NTSC)	-5	0	5	ns
t_{SKEW}	Skew Between Y_{OUT} and C_{OUT}[2]	at 1MHz	-2	0	2	ns
t_{CLGCV}	Chroma-Luma Gain CV_{OUT}[1]	f = 3.58MHz (ref to Y_{IN} at 400kHz)	98	100	102	%
t_{CLDCV}	Chroma-Luma Delay CV_{OUT}[1]	f = 3.58MHz (ref to Y_{IN} at 400kHz)	-10	0	10	ns
GD_{EQ}	Group Delay EQ_NOTCH[1]	f = 3.58MHz (ref to Y_{IN} at 400kHz)	-195	-180	-165	ns
t_{CLGEQ}	Chroma-Luma Gain EQ_NOTCH[1]	f = 3.58MHz (ref to Y_{IN} at 400kHz)	95	100	105	%
t_{CLDEQ}	Chroma-Luma Delay EQ_NOTCH[1]	f = 3.58MHz (ref to Y_{IN} at 400kHz)	-195	-180	-165	ns
dG_{EQ}	Differential Gain[2]	EQ_NOTCH Channel		0.3	1	%
$d\theta_{EQ}$	Differential Phase[2]	EQ_NOTCH Channel		0.3	0.75	%
MCF	Modulator Channel Flatness[1,3]	EQ_NOTCH from 400kHz to 3.75MHz	-0.5	0	0.5	dB
AV_{PK}	Gain Peaking[1]	EQ_NOTCH from >3.75MHz to 4.2MHz	-0.5	0	0.5	dB
Atten1	Notch Attenuation 1[1]	EQ_NOTCH at 4.425MHz	14			dB
Atten2	Notch Attenuation 2[1]	EQ_NOTCH at 4.5MHz	20			dB
Atten3	Notch Attenuation 3[1]	EQ_NOTCH at 4.6MHz	14			dB
t_{PASS}	Passband Group Delay, EQ_NOTCH[1]	f = 400kHz to f = 3MHz	-35		35	ns

Notes:
1. 100% tested at 25°C.
2. Guaranteed by characterization.
3. Tested down to 400kHz, but guaranteed by design to 200kHz.
4. Sustained short circuit protection limited to 10 seconds.

Typical Performance Characteristics

T_c = 25°C, V_i = 1V_{pp}, V_{CC} = 5V, all inputs AC-coupled with 0.1µF, all outputs are AC-coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted.

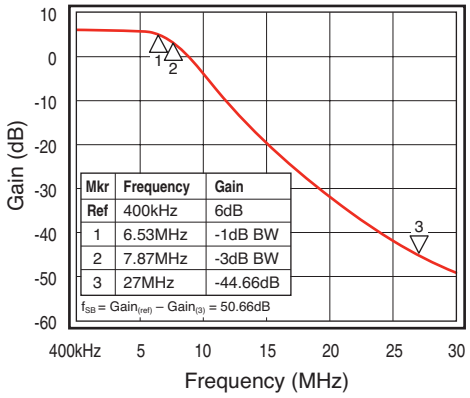


Figure 1. Frequency Response Y_{OUT}

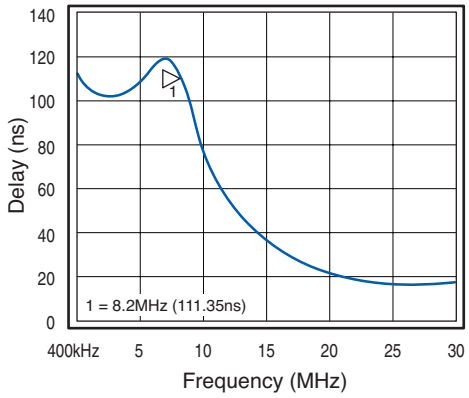


Figure 2. Group Delay vs. Frequency Y_{OUT}

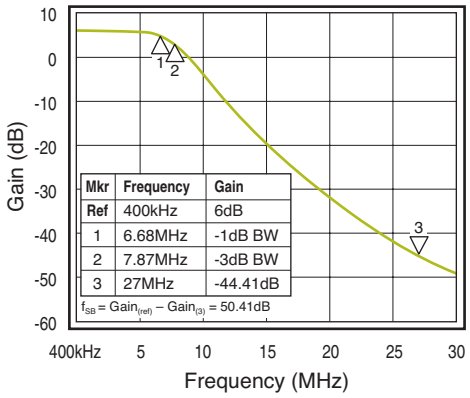


Figure 3. Frequency Response C_{OUT}

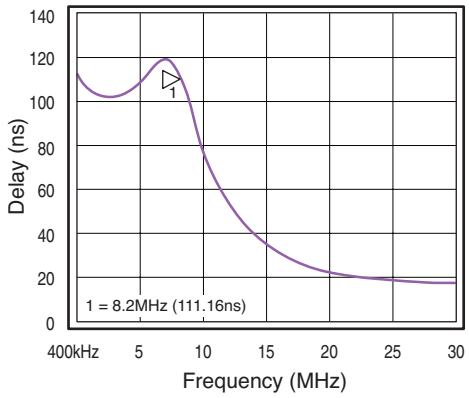


Figure 4. Group Delay vs. Frequency C_{OUT}

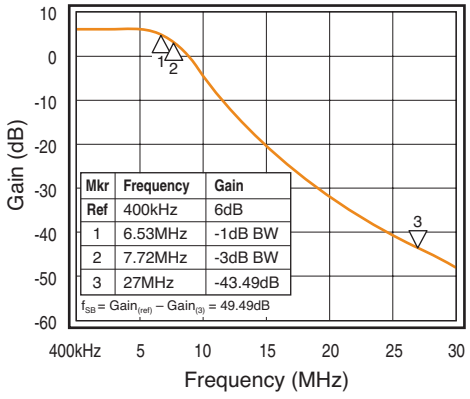


Figure 5. Frequency Response CV_{OUT}

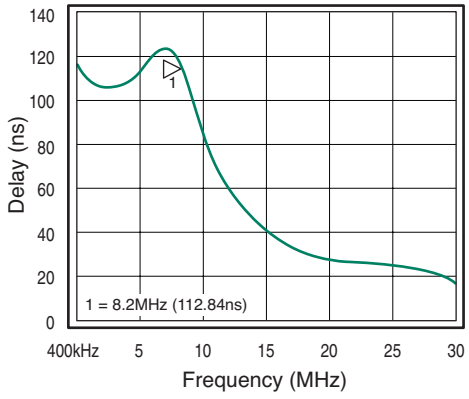


Figure 6. Group Delay vs. Frequency CV_{OUT}

Typical Performance Characteristics

T_c = 25°C, V_i = 1V_{pp}, V_{CC} = 5V, HD/N_SD = 0, R_{SOURCE} = 37.5Ω, all inputs AC-coupled with 0.1µF, all outputs are AC-coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted.

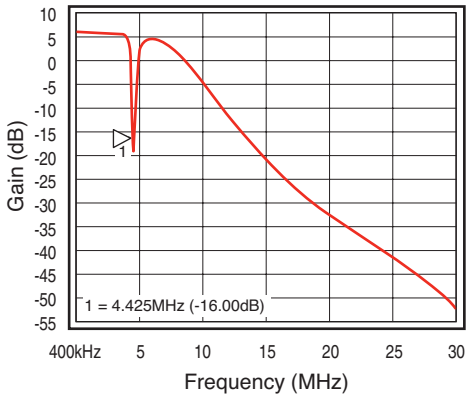


Figure 7. Modulator vs. Frequency Response

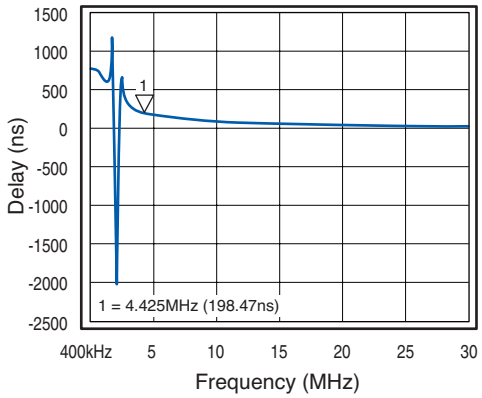


Figure 8. Delay Modulator Output

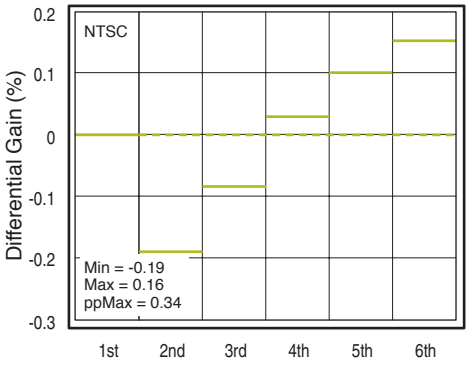


Figure 9. Differential Gain, MOD_{OUT}

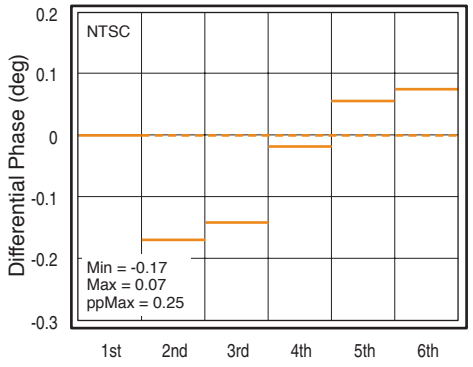


Figure 10. Differential Phase, MOD_{OUT}

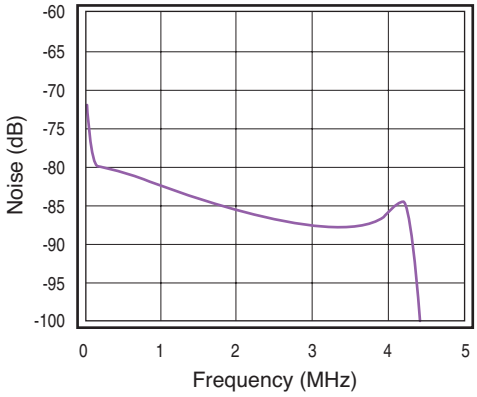


Figure 11. Noise vs. Freq. Modulator Channel

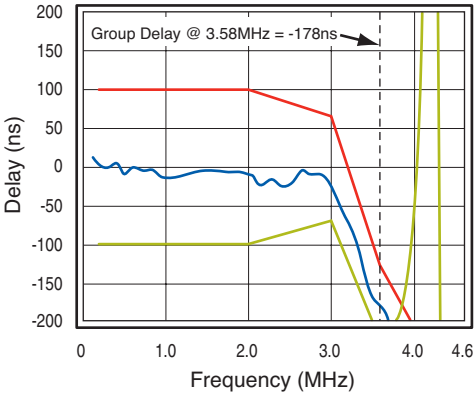


Figure 12. Group Delay vs. Frequency

Typical Performance Characteristics

T_c = 25°C, V_i = 1V_{pp}, V_{CC} = 5V, HD/N_SD = 0, R_{SOURCE} = 37.5Ω, all inputs AC-coupled with 0.1µF, all outputs are AC-coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted.

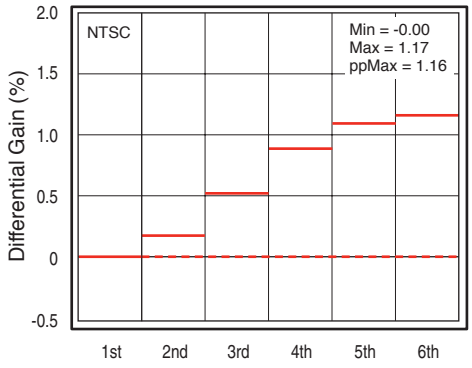


Figure 13. Differential Gain, V_{OUT}

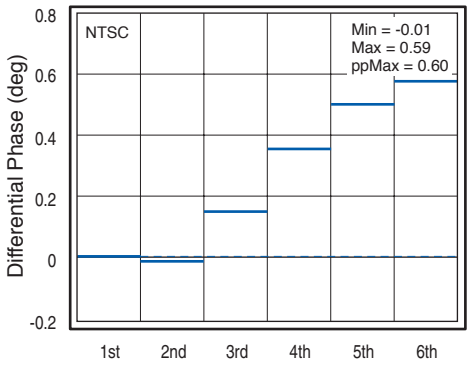


Figure 14. Differential Phase, V_{OUT}

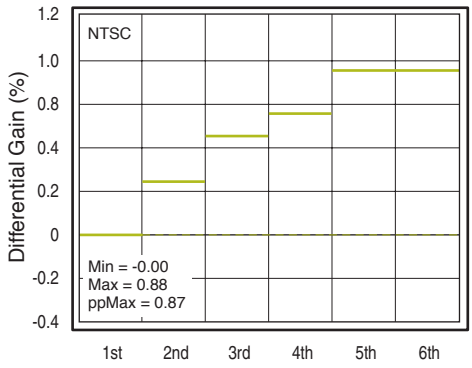


Figure 15. Differential Gain, C_{OUT}

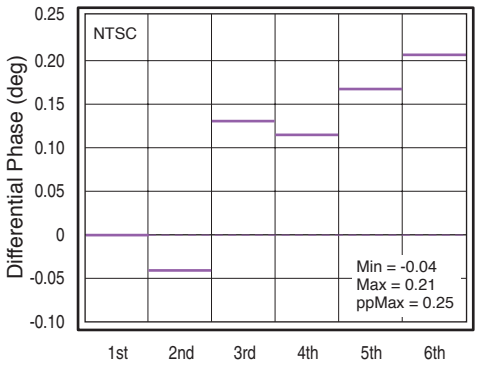


Figure 16. Differential Phase, C_{OUT}

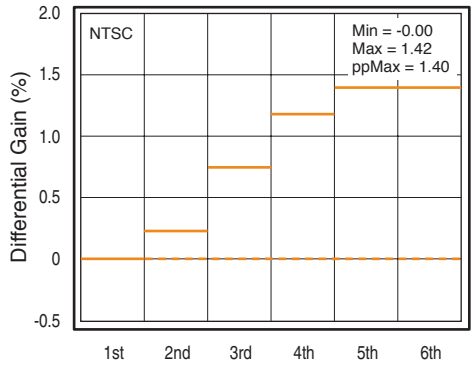


Figure 17. Differential Gain, CV_{OUT}

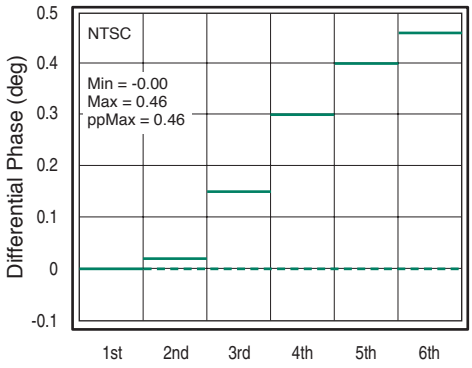


Figure 18. Differential Phase, CV_{OUT}

Typical Performance Characteristics

T_c = 25°C, V_i = 1V_{pp}, V_{CC} = 5V, HD/N_SD = 0, R_{SOURCE} = 37.5Ω, all inputs AC-coupled with 0.1µF, all outputs are AC-coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted.

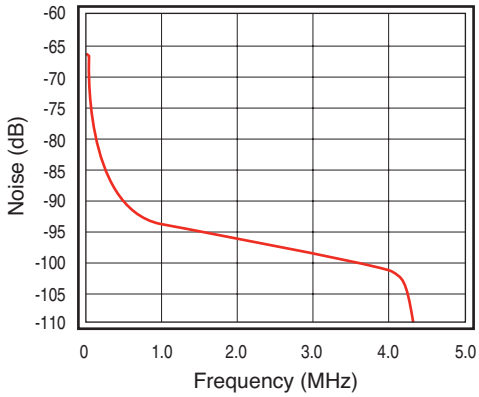


Figure 19. Noise vs. Frequency Y_{OUT}

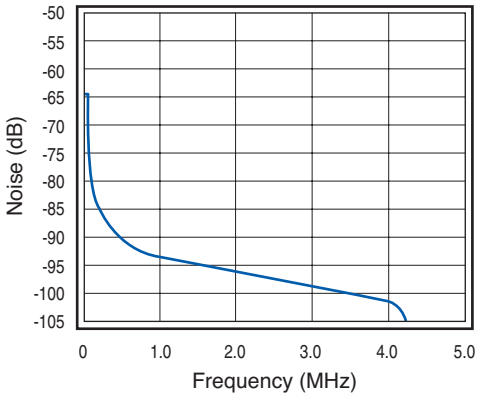


Figure 20. Noise vs. Frequency C_{OUT}

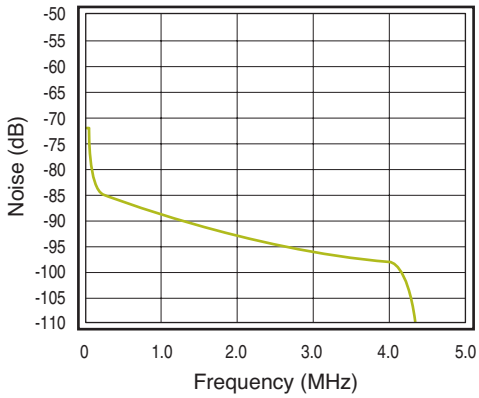


Figure 21. Noise vs. Frequency CV_{OUT}

Typical Application Diagrams

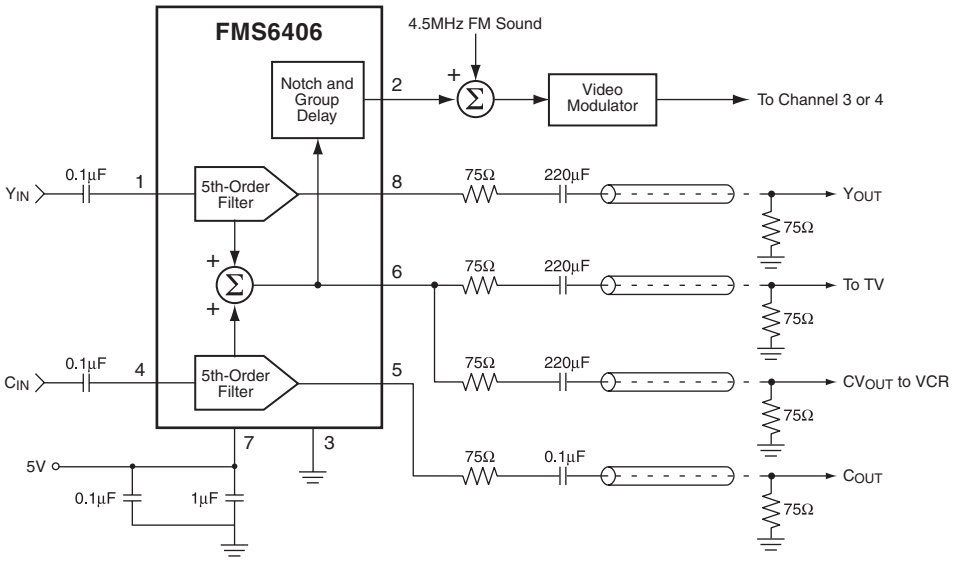


Figure 22. AC-Coupled Application Diagram

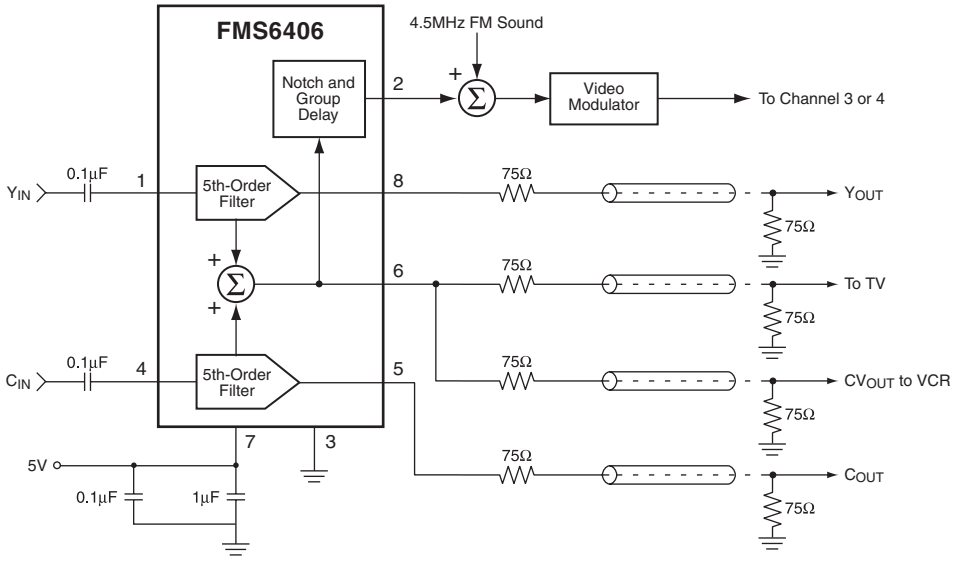


Figure 23. DC-Coupled Application Diagram

Functional Description

Introduction

This product is a two channel monolithic continuous time video filter designed for reconstructing the luminance and chrominance signals from an S-Video D/A source. Composite video output is generated by summing the Y and C outputs. The chip is designed to have AC coupled inputs and will work equally well with either AC or DC coupled outputs.

The reconstruction filters provide a 5th-order Butterworth response with group delay equalization. This provides a maximally flat response in terms of delay and amplitude. Each of the four outputs is capable of driving $2V_{pp}$ into a 75Ω load.

All channels are clamped during the sync interval to set the appropriate minimum output DC level. With this operation the effective input time constant is greatly reduced, which allows for the use of small low cost coupling capacitors. The net effect is that the input will settle to 10mV in 5ms for any DC shifts present in the input video signal.

In most applications the input coupling capacitors are 0.1µF. The Y and C inputs typically sink 1µA of current during active video, which normally tilts a horizontal line by 2mV at the Y output. During sync, the clamp restores this leakage current by sourcing an average of 20µA over the clamp interval. Any change in the coupling capacitor values will affect the amount of tilt per line. Any reduction in tilt will come with an increase in settling time.

Luminance (Y) I/O

The typical luma input is driven by either a low impedance source of $1V_{pp}$ or the output of a 75Ω terminated line driven by the output of a current DAC. In either case, the input must be capacitively coupled to allow the sync-detect and DC restore circuitry to operate properly.

All outputs are capable of driving $2V_{pp}$, AC or DC-coupled, into either a single or dual video load. A single video load consists of a series 75Ω impedance matching resistor connected to a terminated 75Ω line, this presents a total of 150Ω of loading to the part. A dual load would be two of these in parallel which would present a total of 75Ω to the part. The gain of the Y, C and CV signals is 6dB with $1V_{pp}$ input levels. Even when two loads are present the driver will produce a full $2V_{pp}$ signal at its output pin.

Chrominance (C) I/O

The chrominance input can be driven in the same manner as the luminance input but is typically only a $0.7V_{pp}$ signal.

Since the chrominance signal doesn't contain any DC content, the output signal can be AC coupled using as small as a 0.1µF capacitor if DC-coupling is not desired.

Composite Video (CV) Output

The composite video output driver is same as the other outputs. When driving a dual load either output will still function if the other output connection is inadvertently shorted providing these loads are AC-coupled.

Equalizer/Notch (EQ_NOTCH) Output

This output is designed to drive a 600Ω load to $2V_{pp}$, which will meet its primary intention of driving a modulator load.

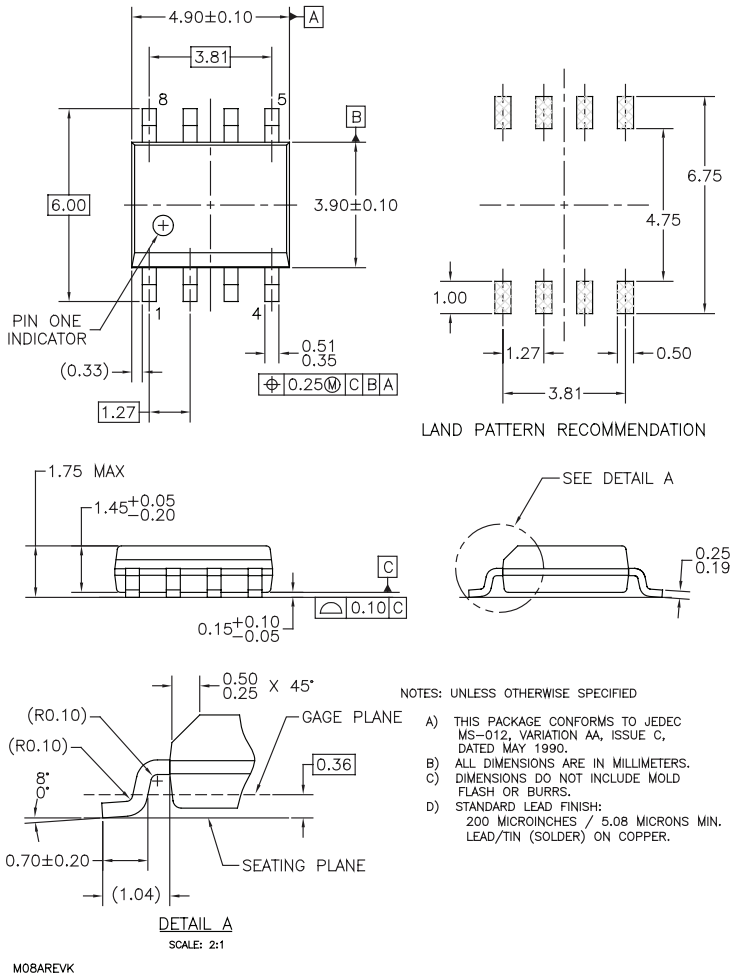
Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance and thermal characteristics. The FMS6406DEMO is a 4-layer board with a full power and ground plane. Following this layout configuration will provide the optimum performance and thermal characteristics. For optimum results, follow the steps below as a basis for high frequency layout:

- Include 1µF and 0.1µF ceramic bypass capacitors
- Place the 1µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- For multi-layer boards, use a large ground plane to help dissipate heat
- For 2-layer boards, use a ground plane that extends beyond the device by at least 0.5”
- Minimize all trace lengths to reduce series inductances

Mechanical Dimensions

8-Lead Outline Package (SOIC)



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS–012, VARIATION AA, ISSUE C, DATED MAY 1990.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) STANDARD LEAD FINISH: 200 MICROINCHES / 5.08 MICRONS MIN. LEAD/TIN (SOLDER) ON COPPER.

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Build it Now™	FRFET™	MicroFET™	QFET®	SuperSOT™-8
CoolFET™	GlobalOptoisolator™	MicroPak™	QS™	SyncFET™
CROSSVOLT™	GTO™	MICROWIRE™	QT Optoelectronics™	TCM™
DOME™	HiSeC™	MSX™	Quiet Series™	TinyLogic®
EcoSPARK™	I^2C™	MSXPro™	RapidConfigure™	TINYOPTO™
E^2CMOS™	*i-Lo*™	OCX™	RapidConnect™	TruTranslation™
EnSigna™	ImpliedDisconnect™	OCXPro™	µSerDes™	UHC™
FACT™	IntelliMAX™	OPTOLOGIC®	ScalarPump™	UniFET™
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